IEEE *Draft* P802.3ab/D1.1

Supplement to: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method & Physical Layer Specifications:

Physical layer specification for 1000 Mb/s operation on four pairs of Category 5 or better balanced twisted pair cable (1000BASE-T)

Sponsor

LAN MAN Standards Committee
of the
IEEE Computer Society

This is the text approved by the 802.3ab task force at its plenary meeting in Montreal, November 1997 as a draft supplement to IEEE Std 802.3 that provides support for 1000 Mb/s operation over four pair of Category 5 or better balanced cabling. This draft D1.1 includes changes and corrections made by the 802.3ab editor and sub-editors as per direction received at the 802.3ab November 1997 plenary meeting. This draft D1.1 is being circulated for task force review. The formal expiration date of this draft is March, 1998.

40 Physical coding sublayer (PCS), physical medium attachment (PMA) sublayer and baseband medium, type 1000BASE-T

40.1 Overview

The 1000BASE-T PHY is one of the 100BASE-T family of high-speed CSMA/CD network specifications. The 1000BASE-T Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) and baseband medium specifications are aimed at users who want 1000 Mb/s performance over data grade category 5 twisted pair cabling systems. 1000BASE-T signaling requires four pairs of category 5 cabling or cabling with better transfer characteristics than category 5, installed according to ANSI/EIA/TIA-568-A, as specified in 40.8. This type of cabling, and the connectors used with it, are simple to install and reconfigure.

This clause defines the type 1000BASE-T PCS, type 1000BASE-T PMA sublayer and type 1000BASE-T Medium Dependent Interface (MDI). Together, the PCS and the PMA sublayer comprise a 1000BASE-T Physical layer (PHY). Control actions needed for correct PHY operations are specified by the 1000BASE-T PHY Control function. Provided in this document are full functional, electrical and mechanical specifications for the type 1000BASE-T PHY Control function, PCS, PMA and MDI. This clause also specifies the baseband medium used with 1000BASE-T.

The following are the objectives of 1000BASE-T PHY, developed and approved by the IEEE 802.3 1000BASE-T Study Group in November, 1996. These requirements were used to drive the definition of the transmission and coding system for the 1000BASE-T standard:

a) Comply with specifications for GMII of 802.3z.
b) Provide line transmission which supports full and half duplex operation.
c) Must provide FCC Class A/CISPR or better operation
d) Support operation over 100 meters of Category 5 cabling
e) Bit Error Rate of less than or equal to 10^{-10}
f) Support Auto-Negotiation (Clause 28)
g) Identify appropriate susceptibility requirements
h) Support the objectives of 802.3z as of 13 November 96

40.1.1 Relation of 1000BASE-T to other standards

Relations between the 1000BASE-T PHY and the ISO Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 CSMA/CD LAN Model are shown in figure 40-1. The PHY layers shown in figure 40-1 connect one clause 4 Media Access Control (MAC) layer to a clause 27 repeater. This clause also discusses other variations of the basic configuration shown in figure 40-1. This whole clause builds on clauses 1-4, 21, 22, 27, 30, 31, 35, 41 and 42 of this standard.

40.1.2 Operation of 1000BASE-T

The 1000BASE-T PHY employs full-duplex baseband transmission over four pairs of Category 5 Unshielded twisted-pair (UTP-5) wiring. The aggregate data rate of 1000 Mb/s is achieved by transmission at a data rate of 250 Mb/s over each wire pair, as shown in figure 40-2. The use of hybrids and echo cancellers enable full-duplex transmission by allowing symbols to be transmitted and received on the same wire pairs at the same time. Baseband signalling with a modulation rate of 125Mbaud is used on each of the wire-pairs. The transmitted symbols are selected from a four-dimensional 5 level symbol constellation. Each four-dimensional symbol can be viewed as a 4-tuple (A_n, B_n, C_n, D_n) of one-dimensional quinary symbols taken from the set {-2, -1, 0, +1, +2}. Five-level Pulse Amplitude Modulation is employed for transmission over each wire pair (PAM5). The modulation rate of 125 MBd matches the GMII clock rate of 125 MHz and

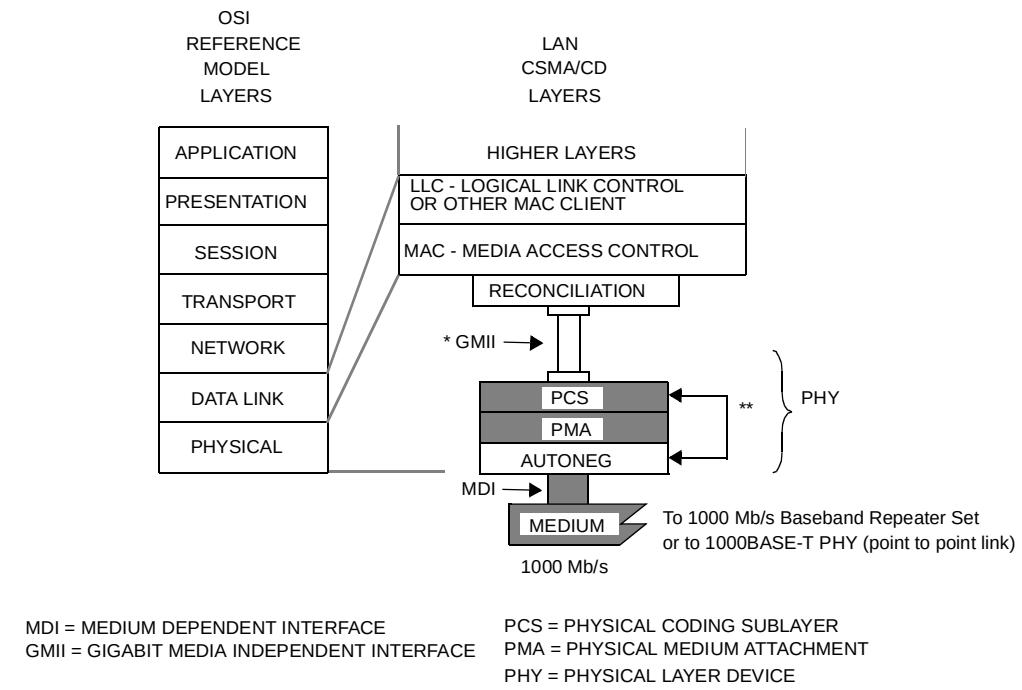


Figure 40-1—Type 1000BASE-T PHY relationship to the ISO Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 CSMA/CD LAN Model

results in a symbol period of 8 ns. This specification permits the use of category 5 or better balanced cable pairs, installed according to ANSI/TIA/EIA-568-A. Thus, 1000BASE-T uses methods already used in two IEEE standards, 100BASE-TX (125Mbaud baseband signaling) and 100BASE-T2 (PAM5). This was chosen to make the 1000BASE-T PHY more 100BASE-T friendly for 100/1000 dual-speed Ethernet PHY implementations, and to make the standards development less time-consuming.

A 1000BASE-T PHY can be configured either as a *master* PHY or as a *slave* PHY. The master-slave relationship between two stations sharing a link segment is established during Auto-Negotiation (see clause 28, 40.6, and Annex 28C). The master PHY uses an external clock to determine the timing of transmitter and receiver operations. The slave PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations, i.e., it performs loop timing, as illustrated in figure 40-3. In a DTE to repeater connection, the repeater is typically set to be master and the DTE is typically set to be slave.

The following paragraphs summarize the PCS, PMA, and PHY Control sections of this document. figure 40-3 shows the division of responsibilities between the PCS, the PMA sublayer, and the PHY Control function.

.

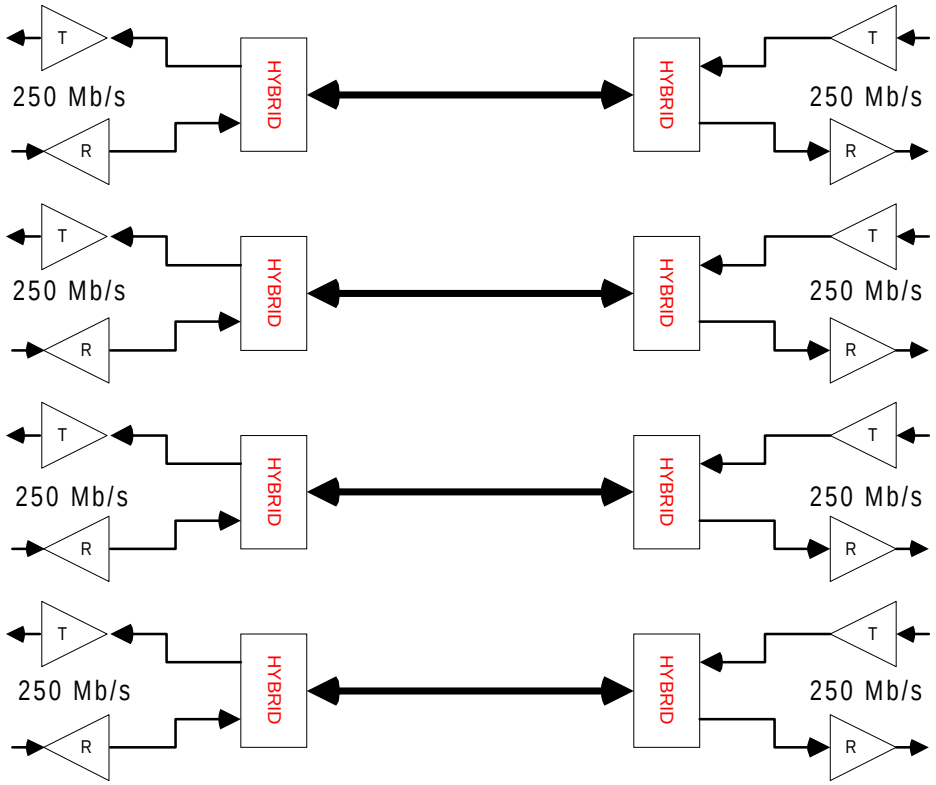


Figure 40-2—1000BASE-T topology

40.1.2.1 Physical coding sublayer (PCS)

The 1000BASE-T2 PCS couples a Gigabit Media Independent Interface (GMII), as described in clause 35, to a Physical Medium Attachment (PMA) sublayer.

The functions performed by the PCS comprise the generation of continuous quinary symbol sequences to be transmitted over each wire pair. During data mode, i.e., when a data stream from the GMII is transmitted, the eight bits representing the TXD<7:0> data octet are encoded into four quinary symbols. During idle mode, i.e., between transmission of consecutive data streams, the sequences of quinary symbols are generated with an encoding rule that differs from the encoding rule used in data mode. Through this technique, sequences of arbitrary quinary symbols that represent data can easily be distinguished from sequences that represent the idle mode. Furthermore, idle mode encoding takes into account the information of whether the local PHY is operating reliably or not and allows conveying this information to the remote station. A transition from the idle to the data mode is signaled by inserting a Start-of-Stream delimiter that consists of a pattern of two consecutive pairs of quinary symbols. Similarly, the end of a data stream transmission is signaled by inserting an End-of-Stream delimiter that also consists of a pattern of two consecutive pairs of quinary symbols. Further patterns are reserved for signaling a transmit error during transmission of a data stream.

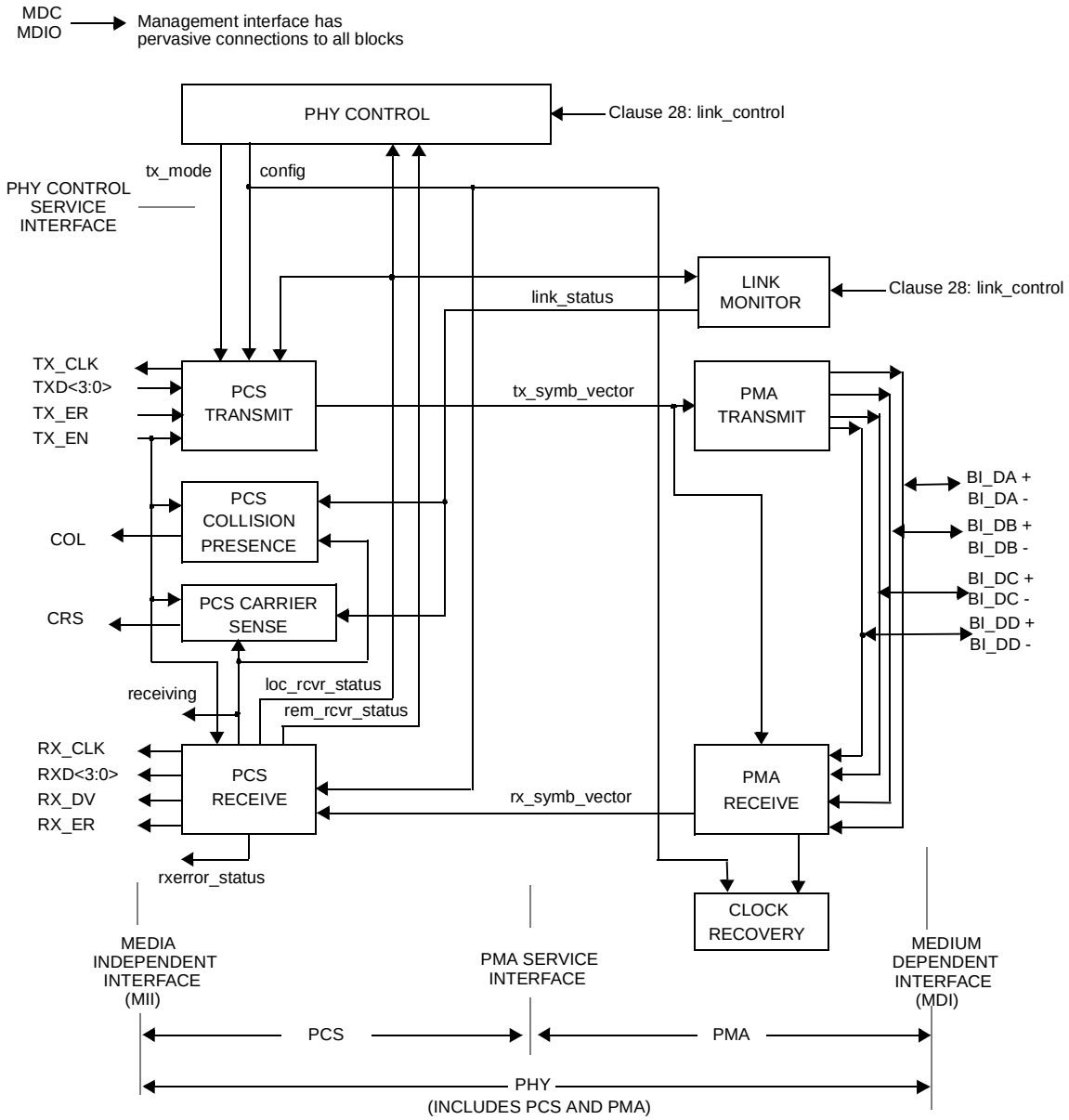


Figure 40-3—Division of responsibility between 1000BASE-T PCS and PMA

PCS Receive processes symbol sets provided by the PMA. It detects the beginning and the end of streams of data and, during the reception of a data stream, descrambles and decodes the received symbols into octets RXD<7:0> that are passed to the GMII. PCS Receive also detects errors in the received sequences and signals them to the GMII. Furthermore, the PCS contains a PCS Carrier Sense function, a PCS Collision Presence function, and a management interface.

The PCS functions and state diagrams are specified in 40.4. The signals provided by the PCS at the GMII conform to the interface requirements of clause 35. The PCS interfaces to PHY Control and to the PMA are abstract message-passing interfaces specified in 40.4.2 and 40.5.2, respectively.

40.1.2.2 Physical medium attachment (PMA) sublayer

The PMA couples messages from the PMA service interface onto the balanced cabling physical medium. The PMA provides dual-duplex communications at 125 MBd over four pairs of balanced cabling up to 100 meters in length.

The PMA Transmit function comprises four independent transmitters to generate five-level pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, DI_DC, and BI_DD, as described in 40.5.1.2.1.

The PMA Receive function comprises four independent receivers for five-level pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, DI_DC, and BI_DD, as described in 40.5.1.2.2. The receivers are responsible for acquiring clock, and providing quinary symbol pairs to the PCS as defined by the PMA_UNITDATA.indicate message. The PMA also contains functions for Link Monitor.

PMA functions and state diagrams are specified in 40.5. PMA electrical specifications are given in 40.7.

40.1.2.3 PHY Control function

PCS and PMA sublayer operations are controlled via signals generated by the PHY Control function. PHY Control does not itself represent a sublayer but rather a logical grouping of the control functions necessary for proper operations of a 1000BASE-T transceiver.

PHY Control determines whether the PHY should operate in a normal state, where packets can be exchanged over the link segment, or whether the PHY should be forced to send quinary symbol sequences that represent the idle mode. The latter occurs when either one of the PHYs, or both PHYs, that share a link segment are not operating reliably.

The PHY Control function and state diagram are specified in 40.3., prior to introducing the PCS and PMA functional specifications. The PHY Control interface to the PCS and PMA sublayer is an abstract message-passing interface also specified in 40.3.

40.1.3 Application of 1000BASE-T

40.1.3.1 Compatibility considerations

All implementations of the balanced cabling link shall be compatible at the MDI. The PCS, PMA and the medium are defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided the MDI and GMII specifications are met.

40.1.3.2 Incorporating the 1000BASE-T PHY into a DTE

When the PHY is incorporated within the physical bounds of a DTE, conformance to the GMII is optional, provided that the observable behavior of the resulting system is identical to that of a system with a full GMII implementation. For example, an integrated PHY may incorporate an interface between PCS and MAC that is logically equivalent to the GMII, but does not have the full output current drive capability called for in the GMII specification.

40.1.3.3 Use of 1000BASE-T PHY for point-to-point communication

The 1000BASE-T PHY, in conjunction with the MAC specified in clauses 1-4 (including parameterized values in 4.4.2.3 to support 1000 Mb/s operation) may be used at both ends of a link for point-to-point applica-

tions between two DTEs. Such a configuration does not require a repeater. In this case each PHY may connect through an GMII to its respective DTE. Optionally, either PHY (or both PHYs) may be incorporated into the DTEs without an exposed GMII.

40.1.3.4 Auto-Negotiation requirement

Full Auto-Negotiation, as specified in clause 28, shall be included in all compliant implementations.

40.1.4 State diagram conventions

The body of this clause and its associated annexes contain state diagrams, including definitions of variables, constants and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram shall prevail. The notation used in the state diagrams follows the conventions of 21.5.

40.2 Signaling

Signaling for 1000BASE-T is performed in the Physical Coding Sublayer (PCS), which generates continuous quinary symbol sequences that are passed to the PMA for transmission over each wire pair. The signaling scheme achieves a number of objectives including:

a) Gray-coded symbol mapping for data
b) uncorrelated symbols in the transmitted symbol stream
c) no correlation between symbol streams travelling both directions on a single pair
d) no correlation between symbol streams on pairs A, B, C and D
e) no correlation between symbol streams on adjacent services in the same cable bundle
f) identical distribution of symbols in data and idle modes
g) ability to rapidly or immediately determine if a symbol stream represents data or idle
h) robust delimiters for SSD, ESD, and other control signals
i) ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining
j) ability of the implementor to utilize available training algorithms

The PCS operates in two basic modes, normal mode or training mode. In normal mode, the tx_mode parameter is set to SEND_N by the PHY Control function, and the PCS generates symbols sequences that representing data or idle streams. In training mode, the transmitter is disabled from sending data, and it is directed by PHY Control to send idle symbols (when tx_mode = SEND_I) which enables the receiver at the other end to train until it is ready to operate in normal mode. The PCS reference diagram is shown in figure 40-5.

40.3 PHY Control functional specifications and service interface

40.3.1 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY in a mode of operation during which packets can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in figure 40-4.

During Auto-Negotiation, PHY Control ensures that the transmitter is disabled. When the Auto-Negotiation process asserts link_control=ENABLE, PHY Control enters the SLAVE DFE CONVERGENCE state. During this state, the actions of PHY Control are dependent upon whether the PHY operates in Master mode or in Slave mode, but the PHY Control enforces transmission of zeros by setting tx_mode=SEND_Z. If in Master mode, the PHY asserts loc_rcvr_status = RNOK and enters the MASTER ECHO CONVERGENCE state immediately. In Slave mode, the PHY asserts loc_rcvr_status = RNOK and enters the SLAVE ECHO CONVERGENCE state only after it performs acquisition of initial adaptive filter parameters as desired.

In either ECHO CONVERGENCE states, PHY Control enforces transmission in the idle mode by setting tx_mode=SEND_I and the PHY transmits sequences of ternary symbols. When the PHY detects valid 1000BASE-T signal reception from the remote PHY, it transitions out of these states. In Master mode, the PHY enters the MASTER DFE CONVERGENCE state and PHY CONTROL enforces transmission of zeros by setting tx_mode=SEND_Z. After the Master PHY performs acquisition of initial adaptive filter parameters as desired, the PHY asserts loc_rcvr_status=RNOK and enters the TRAINING state. In Slave mode, the PHY enters the TRAINING state directly from its ECHO CONVERGENCE state.

The TRAINING state is where the final convergence of the adaptive filter parameters and the timing acquisition is completed. After the PHY completes successful training and establishes proper receiver operations, PCS Receive asserts the parameter loc_rcvr_status=OK, and PCS Transmit conveys this information to the link partner via ternary transmission. The criterion for setting the parameter loc_rcvr_status is left to the implementor. It can be based, for example, on observing the mean-square error at the decision point of the receiver or detecting errors during reception of symbol streams that represent the idle mode. Upon observation that the remote PHY also operates reliably (rem_rcvr_status=OK), the normal mode of operation is entered where transmission of packets over the link segment can take place.

The normal mode of operation corresponds to the SEND IDLE OR DATA state, where PHY Control asserts tx_mode=SEND_N. In this state, when no packets have to be sent, idle mode transmission takes place.

If during the normal mode of operation unsatisfactory receiver operation is detected (loc_rcvr_status=RNOK), transmission of the current packet, if any, is completed and PHY Control enters the TRAINING state. If unsatisfactory clock recovery operation is detected (loc_rcvr_status=TNOK), transmission of the current packet, if any, is completed and PHY Control enters the SLAVE DFE CONVERGENCE state.

Whenever a PHY that operates reliably detects unsatisfactory operation of the remote PHY (rem_rcvr_status=NOT_OK), it enters the SEND IDLE state where tx_mode=SEND_I is asserted and idle transmission takes place. In this state, encoding is performed with the parameter loc_rcvr_status = OK. As soon as the remote PHY signals satisfactory receiver operation (rem_rcvr_status=OK), the SEND IDLE OR DATA state is entered. Note that if in the SEND IDLE state loc_rcvr_status takes the value RNOK, transition to the TRAINING state occurs, and if loc_rcvr_status takes the value TNOK, transition to the SLAVE DFE CONVERGENCE state occurs.

PHY Control may force the transmit scrambler state to be initialized to an arbitrary value by requesting the execution of the PCS Reset function defined in 40.4.1.1.

40.3.2 PHY Control Service interface

The following specifies the services provided by PHY Control. These services are described in an abstract manner and do not imply any particular implementation.

The following primitives are defined:

PHYC_CONFIG.indicate

PHYC_CODING.indicate

PHYC_TXMODE.indicate

PHYC_RXSTATUS.request

PHYC_REMRXSTATUS.request

The parameter link_control is identical to the link_control parameter defined for the PMA Service interface in 40.5.2.4.

40.3.2.1 PHYC_CONFIG.indicate

Each PHY in a 1000BASE-T link is configured as a master PHY or as a slave PHY. Master/slave configuration is determined during Auto-Negotiation (40.6). The result of this negotiation is provided to PHY Control.

40.3.2.1.1 Semantics of the primitive

PHYC_CONFIG.indicate (config)

PHYC_CONFIG.indicate specifies to PCS and PMA Clock Recovery via the parameter config whether the PHY must operate as a master PHY or as a slave PHY. The parameter config can take on one of two values of the form:

MASTER	This value is continuously asserted when the PHY must operate as a master PHY.
SLAVE	This value is continuously asserted when the PHY must operate as a slave PHY.

40.3.2.1.2 When generated

PHY Control shall generate PHYC_CONFIG.indicate messages synchronously with every GMII RX_CLK cycle.

40.3.2.1.3 Effect of receipt

Upon reception of this primitive, PCS and PMA Clock Recovery shall perform their functions in master or slave configuration according to the value assumed by the parameter config.

40.3.2.2 PHYC_CODING.indicate

Each PHY in a 1000BASE-T link can employ a convolutional decoder in the receiver in order to improve its Bit Error Rate performance. The PCS Transmit function shall be capable of convolutionally encoding the data stream as per the link partner's decoding ability. The link partner's decoding ability is determined during Auto-Negotiation (40.6). The result of this negotiation is provided to PHY Control.

40.3.2.2.1 Semantics of the primitive

PHYC_CODING.indicate (coding_enable)

PHYC_CODING.indicate specifies to PCS via the parameter coding_enable whether the PHY must use a three-state convolutional encoder or not. The parameter coding_enable can take on one of two values of the form:

ON	This value is continuously asserted when the PHY must enable convolutional encoding.
OFF	This value is continuously asserted when the PHY must disable convolutional encoding.

40.3.2.2.2 When generated

PHY Control shall generate PHYC_CODING.indicate messages synchronously with every GMII RX_CLK cycle.

40.3.2.2.3 Effect of receipt

Upon reception of this primitive, PCS shall perform its encoding functions according to the value assumed by the parameter coding_enable.

40.3.2.3 PHYC_TXMODE.indicate

The transmitter in a 1000BASE-T link normally sends over the four pairs, quinary symbols that can represent an GMII data stream or the idle mode.

40.3.2.3.1 Semantics of the primitive

PHYC_TXMODE.indicate (tx_mode)

PHYC_TXMODE.indicate specifies to PCS Transmit via the parameter tx_mode what sequence of quinary symbols the PCS should be transmitting. The parameter tx_mode can take on one of three values of the form:

SEND_N	This value is continuously asserted when transmission of sequences of quinary symbols representing an GMII data stream or the idle mode is to take place.
SEND_I	This value is continuously asserted in case transmission of sequences of ternary symbols representing the idle mode is to take place.
SEND_Z	This value is continuously asserted in case transmission of zeros is required.

40.3.2.3.2 When generated

PHY Control shall generate PHYC_TXMODE.indicate messages synchronously with every GMII RX_CLK cycle.

40.3.2.3.3 Effect of receipt

Upon receipt of this primitive, the PCS shall perform its Transmit function as described in 40.4.1.2.

40.3.2.4 PHYC_RXSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the receive link for the local PHY. The parameter loc_rcvr_status conveys to PHY Control and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by PCS Transmit encoding functions.

40.3.2.4.1 Semantics of the primitive

PHYC_RXSTATUS.request (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of three values of the form:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY.
RNOK	This value is asserted whenever operation of the receive link for the local PHY is unreliable, but the receive clock recovery operation may be reliable.
TNOK	This value is asserted whenever operation of the receive link for the local PHY, including the receive clock recovery operation is completely unreliable.

40.3.2.4.2 When generated

PCS Receive shall generate PHYC_RXSTATUS.request messages synchronously with signals received at the Gigabit Media Dependent Interface. It shall prevent that the value of the parameter loc_rcvr_status is modified while TX_EN=1 in order to avoid that a transition from data to idle mode or from idle to data mode occurs while a packet is being presented to the PCS at the GMII.

40.3.2.4.3 Effect of receipt

The effect of receipt of this primitive is specified in 40.3.5 and 40.5.1.3.3.

40.3.2.5 PHYC_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link as communicated by the remote PHY. The parameter rem_rcvr_status conveys to PHY Control the information on whether reliable operation of the remote PHY is detected or not.

40.3.2.5.1 Semantics of the primitive

PHYC_REMRXSTATUS.request (rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK	The receive link for the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

40.3.2.5.2 When generated

The PCS shall generate PHYC_REMRXSTATUS.request messages synchronously with signals received at the GMDI.

40.3.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 40.3.5.

40.3.3 State diagram variables

link_control
: See 40.5.1.3.1.

link_status
: See 40.5.1.3.1.

config
: See 40.3.2.1.1.

signal_detect
: See 40.5.1.3.1.

loc_rcvr_status
: Variable set by the PCS Receive function to indicate correct or incorrect operation of the receive link for the local PHY.

  Values: OK: the receive link for the local PHY is operating reliably,
  RNOK: operation of the receive link for the local PHY is not reliable, but the clock recovery operation may be reliable.
  TNOK: operation of the receive link for the local PHY, including the clock recovery circuit operation, is completely unreliable.

pma_reset
: Allows reset of all PMA functions.

  Values: ON and OFF

  Set by: PMA Reset

rem_rcvr_status
: Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not.

  Values: OK: the receive link for the remote PHY is operating reliably,
  NOT_OK: reliable operation of the receive link for the remote PHY is not detected.

tx_mode
: PCS Transmit shall send quinary symbols according to the value assumed by this variable.

  Values: SEND_N: transmission of sequences of quinary symbols representing a GMII data stream, the idle mode, or control signals shall take place,
  SEND_I: transmission of sequences of ternary symbols representing the idle mode shall take place.
  SEND_Z: transmission of zero symbols shall take place.

40.3.4 State diagram timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where ‘stop x_timer’ is asserted.

maxwait_timer

A timer used to measure the amount of time during which a receiver dwells in the DFE/ECHO CONVERGENCE and TRAINING states. The timer shall expire 750 ms after entering the SLAVE DFE CONVERGENCE state.

minwait_timer

A timer used to measure the amount of time during which a receiver waits in a particular state before being allowed to leave that state. The timer shall expire 128T=1.024 μs after being started.

40.3.5 PHY Control state diagram

.

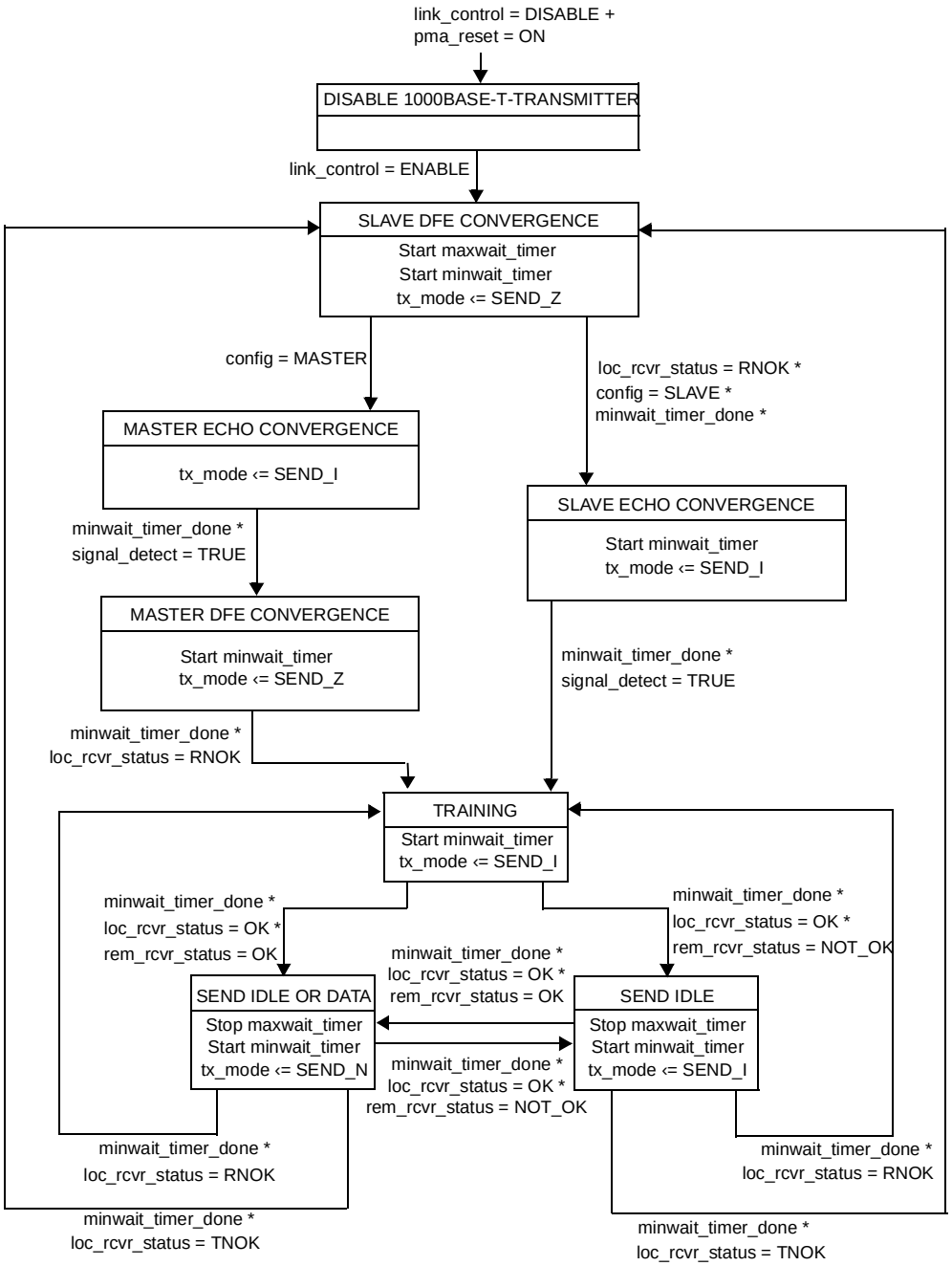


Figure 40-4—PHY Control state diagram

40.4 PCS functional specifications

The PCS comprises one PCS Reset function and four simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit, PCS Receive, PCS Carrier Sense, and PCS Collision Presence. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, figure 40-5, shows how the four operating functions relate to the messages of the PCS-PMA and the PCS-PHY Control interfaces. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive, and are not shown in figure 40-5. The management functions are specified in clause 30. See also figure 40-7, which defines the structure of frames passed from PCS to PMA.

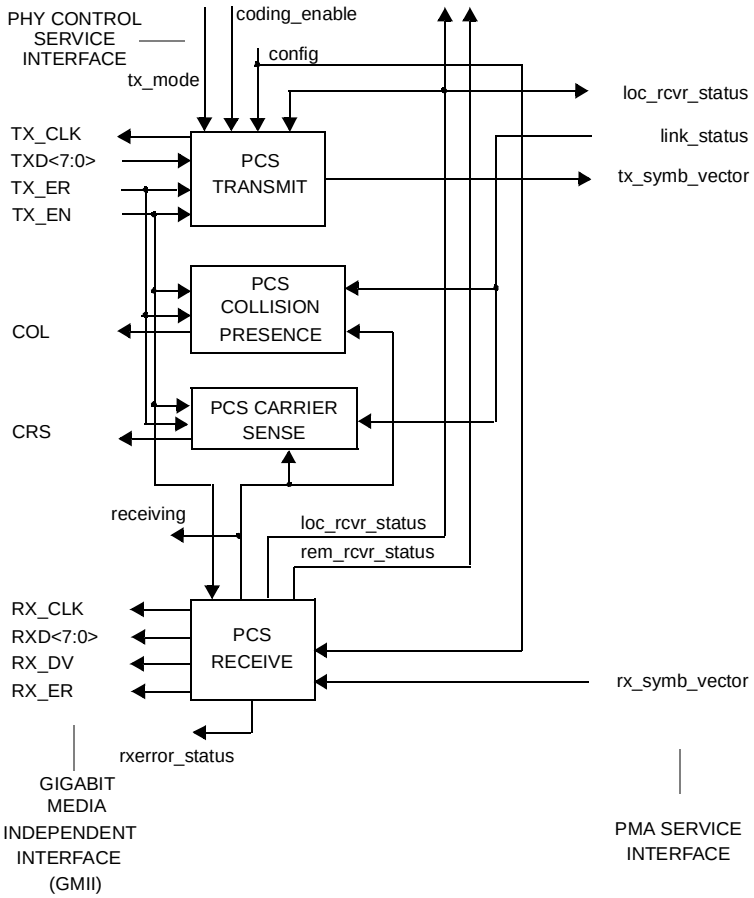


Figure 40-5—PCS reference diagram

40.4.1 PCS functions

40.4.1.1 PCS Reset function

The PCS Reset function shall be executed any time one of three conditions occur. These three conditions are "power on", the receipt of a request for reset from the management entity, and the receipt of a request for

reset from PHY Control. PCS Reset initializes all PCS functions. PCS Reset sets pcs_reset = ON for the duration of its reset function. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

40.4.1.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS Transmit state diagram in figure 40-9.

In normal mode of operation, the tx_mode parameter, which is transferred from PHY Control to the PCS via the PHYC_TXMODE.indicate message, assumes the value tx_mode=SEND_N, and the PCS Transmit function generates at each symbol period pairs of quinary symbols that represent data or the idle mode. A symbol period T is equal to 8 ns. A time index n, where n is an integer, is introduced to establish a temporal relationship between different symbol periods. The tx_symb_vector parameter at time n is a four-element vector of quinary symbols (A_n, B_n, C_n, D_n) that is transferred to the PMA via PMA_UNITDATA.request. The PMA shall transmit symbols A_n, B_n, C_n, and D_n over wire pairs BI_DA, BI_DB, BI_DC, and BI_DD respectively. During transmission of data, the eight bits representing the TXD<7:0> data byte are scrambled by the PCS using a side-stream scrambler, then encoded into a quartet of quinary symbols and transferred to the PMA. During data encoding, the PCS Transmit additionally utilizes a three-state convolutional encoder if the variable coding_enable is ON. The idle mode is signaled by a sequence of quartets of quinary symbols which are also generated using the side-stream transmit scrambler. However, the encoding rules by which the quinary symbols are obtained are different for the data and the idle modes. This allows, at the receiver, sequences of quinary symbol quartets that represent data to be distinguished from sequences of quinary symbol quartets that represent the idle mode. A transition from the idle mode to the data mode is signalled by inserting a Start-of-Stream delimiter that consists of a pattern of two consecutive quartets of quinary symbols. Similarly, the end of transmission of data is signalled by an End-of-Stream delimiter that also consists of a pattern of two consecutive quartets of quinary symbols. Further patterns are reserved for signaling the assertion of TX_ER within a stream of data, Carrier Extension and other control functions.

If tx_mode = SEND_I is asserted, PCS Transmit generates sequences of symbol vectors (A_n, B_n, C_n, D_n) according to the encoding rule in training mode. Training mode encoding takes into account the value of the parameter loc_rcvr_status. By this mechanism, a PHY indicates during idle transmission the status of its own receiver to the link partner.

PCS encoding involves the generation of the four-bit words $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$ from which the quinary symbols (A_n, B_n, C_n, D_n) are obtained. The four-bit words $Sx_n[3:0]$, $Sy_n[3:0]$ and $Sg_n[3:0]$ are determined as explained in 40.4.1.2.2, from sequences of random binary symbols derived from the transmit side-stream scrambler.

40.4.1.2.1 Side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling. If the parameter config provided to the PCS by the PHY Control function via the PHYC_CONFIG.indicate message assumes the value MASTER, PCS Transmit shall employ

$$g_M(x) = 1 + x^{13} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. If config = SLAVE, PCS Transmit shall employ

$$g_S(x) = 1 + x^{20} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. The implementation of master and slave PHY side-stream scramblers by linear-feedback shift registers is shown in figure 40-6. The bits stored in the shift

register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementor.

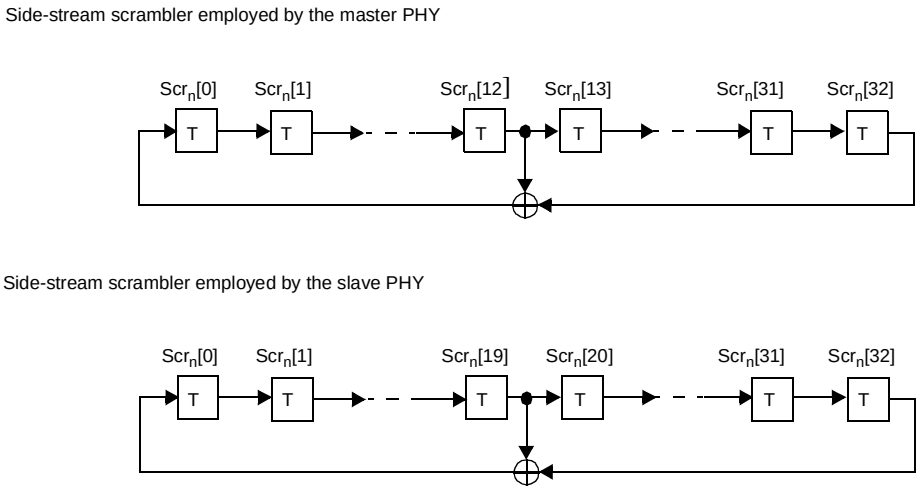


Figure 40-6—Realization of side-stream scramblers by linear feedback shift registers

40.4.1.2.2 Generation of bits $Sx_n[3:0]$, $Sy_n[3:0]$ and $Sg_n[3:0]$

PCS Transmit encoding rules are based on the generation, at time n, of the twelve bits $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$. The eight bits, $Sx_n[3:0]$ and $Sy_n[3:0]$ are used to generate the scrambler byte $Sc_n[7:0]$ for decorrelating the GMII data word Tx_D<7:0> during data transmission and for generating the idle and training symbols. The four bits $Sg_n[3:0]$ are used to randomize the signs of the quinary symbols (A_n, B_n, C_n, D_n) so that each symbol stream has no DC bias. These twelve bits are generated in a systematic fashion using three bits, X_n, Y_n, and $Scr_n[0]$, and an auxiliary generating polynomial, g(x). The two bits, X_n, and Y_n are mutually uncorrelated and also uncorrelated with the bit $Scr_n[0]$. For both master and slave PHYs, they are obtained by the same linear combinations of bits stored in the transmit scrambler shift register delay line. These two bits are derived from elements of the same maximum-length shift register sequence of length $2^{33} - 1$ as $Scr_n[0]$, but shifted in time. The associated delays are all large and different, such that there is no apparent correlation among the bits $Scr_n[0]$, X_n, and Y_n. The bits, X_n, and Y_n are generated as follows

$$X_n = Scr_n[4] \oplus Scr_n[6]$$

$$Y_n = Scr_n[1] \oplus Scr_n[5]$$

where $\oplus$ denotes the XOR logic operator. From the three bits X_n, Y_n, and $Scr_n[0]$, further mutually uncorrelated bit streams are obtained systematically using the generating polynomial

$$g(x) = x^3 \oplus x^8$$

The four bits, $Sy_n[3:0]$ are generated using the bit $Scr_n[0]$ and g(x) as

$$Sy_n[0] = Scr_n[0]$$

$$Sy_n[1] = g(Scr_n[0]) = Scr_n[3] \oplus Scr_n[8]$$

$$Sy_n[2] = g^2(Scr_n[0]) = Scr_n[6] \oplus Scr_n[16]$$

$$Sy_n[3] = g3(Scr_n[0]) = Scr_n[9] \oplus Scr_n[14] \oplus Scr_n[19] \oplus Scr_n[24]$$

The four bits, $Sx_n[3:0]$ are generated using the bit X_n and g(x) as in the following equations.

$$Sx_n[0] = X_n = Scr_n[4] \oplus Scr_n[6]$$

$$Sx_n[1] = g(X_n) = Scr_n[7] \oplus Scr_n[9] \oplus Scr_n[12] \oplus Scr_n[14]$$

$$Sx_n[2] = g^2(X_n) = Scr_n[10] \oplus Scr_n[12] \oplus Scr_n[20] \oplus Scr_n[22]$$

$$Sx_n[3] = g^3(X_n) = Scr_n[13] \oplus Scr_n[15] \oplus Scr_n[18] \oplus Scr_n[20] \oplus Scr_n[23] \oplus Scr_n[25] \oplus Scr_n[28] \oplus Scr_n[30]$$

The four bits, $Sg_n[3:0]$ are generated using the bit Y_n and g(x) as in the following equations.

$$Sg_n[0] = Y_n = Scr_n[1] \oplus Scr_n[5]$$

$$Sg_n[1] = g(Y_n) = Scr_n[4] \oplus Scr_n[8] \oplus Scr_n[9] \oplus Scr_n[13]$$

$$Sg_n[2] = g^2(Y_n) = Scr_n[7] \oplus Scr_n[11] \oplus Scr_n[17] \oplus Scr_n[21]$$

$$Sg_n[3] = g^3(Y_n) = Scr_n[10] \oplus Scr_n[14] \oplus Scr_n[15] \oplus Scr_n[19] \oplus Scr_n[20] \oplus Scr_n[24] \oplus Scr_n[25] \oplus Scr_n[29]$$

By construction, the twelve bits, $Sx_n[3:0]$, $Sy_n[3:0]$ and $Sg_n[3:0]$ are derived from elements of the same maximum-length shift register sequence of length $2^{33} - 1$ as $Scr_n[0]$, but shifted in time by varying delays. The associated delays are all large and different, such that there is no apparent correlation among the bits.

40.4.1.2.3 Generation of bits $Sc_n[7:0]$

The bits $Sc_n[7:0]$ are used to scramble the GMII data byte Tx_D[7:0] and for idle and training mode symbol generation. The definition of these bits is dependent upon the bits $Sx_n[3:0]$, $Sy_n[3:0]$ specified in 40.4.1.2.2, the variable tx_mode obtained through the PHY Control Service Interface, the variable tx_enable_n and the time index, n.If tx_mode = SEND_N and data transmission is enabled as shown in figure 40-8, the encoding rule is determined by the value of the signal tx_enable_n, given by

$$tx\_enable_n = \begin{cases} Tx\_EN_n \text{ if } (data\_transmission\_enabled) \\ 0 \text{ else} \end{cases}$$

where Tx_EN_n represents the GMII signal Tx_EN at time n. Likewise, tx_error_n is defined as Tx_ER_n when data transmission is enabled, where Tx_ER_n represents the GMII signal Tx_ER at time n.

The four bits $Sc_n[7:4]$ are defined as follows

$$Sc_n[7:4] = \begin{cases} Sx_n[3:0] \text{ if } (tx\_enable_n = 1) \\ [\,0\ 0\ 0\ 0\,] \text{ else} \end{cases}$$

The bits $Sc_n[3:1]$ are defined as follows

$$Sc_n[3:1] = \begin{cases} [\,0\ 0\ 0\,] \text{ if (tx\_mode = SEND\_Z)} \\ Sy_n[3:1] \text{ elseif ((loc\_rcvr\_status = OK) and } (n\text{-}n_0) = 0 \text{ (mod 2))} \\ (Sy_{n-1}\,[3:1] \oplus [1\ 1\ 1]) \text{ else} \end{cases}$$

where n_0 denotes the time index of the last transmitter side-stream scrambler reset.

The bit $Sc_n[0]$ is defined as follows

$$Sc_n[0] = \begin{cases} 0 \text{ if (tx\_mode = SEND\_Z)} \\ Sy_n[0] \text{ elseif ((tx\_mode = SEND\_I) or } (n\text{-}n_0) = 0 \text{ (mod 2))} \\ (Sy_{n-1}\,[0] \oplus 1) \text{ else} \end{cases}$$

where n_0 denotes the time index of the last transmitter side-stream scrambler reset.

40.4.1.2.4 Generation of bits $Sd_n[8:0]$

The PCS Transmit function generates a nine-bit word $Sd_n[8:0]$ that represent either a convolutionally encoded stream of data or an idle or training mode word. If $tx\_enable_n = 1$, transmission of a stream of data takes place and the convolutional encoder is used if the variable coding_enable = ON.

The convolutional encoder uses a 3-bit word $cs_n[2:0]$ which is defined as follows

$$cs_n[1] = \begin{cases} Sd_n[6] \oplus cs_{n-1}[0] & \text{if (coding\_enable=ON and } tx\_enable_{n-2} = 1) \\ 0 & \text{else} \end{cases}$$

$$cs_n[2] = \begin{cases} Sd_n[7] \oplus cs_{n-1}[1] & \text{if (coding\_enable=ON and } tx\_enable_{n-2} = 1) \\ 0 & \text{else} \end{cases}$$

$$cs_n[0] = cs_{n-1}[2]$$

from which $Sd_n[8]$ is obtained as

$$Sd_n[8] = cs_n[0]$$

The convolutional encoder bits are non-zero only during the transmission of data. Upon the completion of a data packet, the convolutional encoder bits are reset using the bit $csreset_n$. The bit $csreset_n$ is defined as

$$csreset_n = (tx\_enable_{n-2}) \text{ and } (\text{not } tx\_enable_n)$$

The bits $Sd_n[7:6]$ are derived from the bits $Sc_n[7:6]$, the GMII data bits $Tx\_D_n[7:6]$, and from the convolutional encoder bits as

$$Sd_n[7] = \begin{cases} Sc_n[7] \oplus Tx\_D_n[7] & \text{if } (csreset_n=0 \text{ and } tx\_enable_{n-2} = 1) \\ cs_{n-1}[1] & \text{else if } (csreset_n=1) \\ Sc_n[7] & \text{else} \end{cases}$$

$$Sd_n[6] = \begin{cases} Sc_n[6] \oplus Tx\_D_n[6] & \text{if } (csreset_n=0 \text{ and } tx\_enable_{n-2} = 1) \\ cs_{n-1}[0] & \text{else if } (csreset_n=1) \\ Sc_n[6] & \text{else} \end{cases}$$

The bits $Sd_n[5:2]$ are derived from the bits $Sc_n[5:2]$ and the GMII data bits $Tx\_D_n[5:2]$ as

$$Sd_n[5:2] = \begin{cases} Sc_n[5:2] \oplus Tx\_D_n[5:2] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[5:2] & \text{else} \end{cases}$$

The bits $Sd_n[1:0]$ are used to transmit Carrier Extension information during tx_mode=SEND_N and are thus dependent upon the bits $cext_n$ and $cext\_err_n$. These bits are defined as

$$cext_n = \begin{cases} tx\_error_n & \text{if } ((tx\_enable_n = 0) \text{ and } (Tx\_D_n[7:0] = 0x0F)) \\ 0 & \text{else} \end{cases}$$

$$cext\_err_n = \begin{cases} tx\_error_n \text{ if } ((tx\_enable_n = 0) \text{ and } (Tx\_D_n[7:0] = 0x1F)) \\ 0 \text{ else} \end{cases}$$

$$Sd_n[1] = \begin{cases} Sc_n[1] \oplus Tx\_D_n[1] \text{ if } (tx\_enable_{n-2} = 1) \\ Sc_n[1] \oplus cext\_err_n \text{ else} \end{cases}$$

$$Sd_n[0] = \begin{cases} Sc_n[0] \oplus Tx\_D_n[0] \text{ if } (tx\_enable_{n-2} = 1) \\ Sc_n[0] \oplus cext_n \text{ else} \end{cases}$$

40.4.1.2.5 Generation of Quinary Symbols TA_n, TB_n, TC_n, TD_n

The nine-bit word $Sd_n[8:0]$ is mapped to a quartet of quinary symbols (TA_n, TB_n, TC_n, TD_n) according to table 40-1 and table 40-2.

Encoding of error indication:

If tx_error_n=1 is asserted when the condition (tx_enable_n * tx_enable_{n-2}) = 1, where "*" denotes the logic AND operator, error indication is signaled by means of symbol substitution. In this condition, the values of $Sd_n[5:0]$ are ignored by PCS Transmit and the symbols corresponding to the row denoted as "Xmt_Err" in table 40-1 and table 40-2 shall be used.

Encoding of Convolutional Encoder Reset:

If tx_error_n=0 is asserted when the variable $csreset_n$ = 1, the convolutional encoder reset condition is normal. This condition is indicated by means of symbol substitution, where the values of $Sd_n[5:0]$ are ignored by PCS Transmit and the symbols corresponding to the row denoted as "CSReset" in table 40-1 and table 40-2 shall be used.

Encoding of Carrier Extension during Convolutional Encoder Reset:

If tx_error_n=1 is asserted when the variable $csreset_n$ = 1, the convolutional encoder reset condition must indicate carrier extension. In this condition, the values of $Sd_n[5:0]$ are ignored by PCS Transmit and the symbols corresponding to the row denoted as "CSExtend" in table 40-1 and table 40-2 shall be used when TxD_n = 0x'0F, and the row denoted as "CSExtend_Err" in table 40-1 and table 40-2 shall be used when TxD_n = 0x'1F. The latter condition denotes Carrier Extension with Error. In case Carrier Extension with Error is indicated during the first byte of csreset, the Error condition shall be encoded during the second byte of csreset, and during the subsequent two bytes of the End-of-Stream delimiter as well. Thus, the Error condition is assumed to persist during the symbol substitutions at the End-of-Stream.

Encoding of Start-of-Stream Delimiter:

The Start-of-Stream Delimiter ("SSD") is related to the condition SSD_n = (tx_enable_n) * (! tx_enable_{n-2}) = 1, where "*" and "!" denote the logic AND and NOT operators, respectively. For the generation of "SSD", PCS Transmit replaces the first two bytes of the preamble in a data stream with the symbols corresponding to the rows denoted as SSD1 and SSD2 respectively in table 40-1. The symbols corresponding to the SSD1

row shall be used when the condition (tx_enable_n) * (! tx_enable_{n-1}) = 1. The symbols corresponding to the SSD2 row shall be used when the condition (tx_enable_{n-1}) * (! tx_enable_{n-2}) = 1.

Encoding of End-of-Stream Delimiter:

The definition of an End-of-Stream Delimiter ("ESD") is related to the condition ESD_n= (! tx_enable_{n-2}) * (tn_enable_{n-4}) = 1. This occurs during the third and fourth symbol periods after transmission of the last byte of a data stream.

If Carrier Extend Error is indicated during ESD, that is, when tx_error_n = 1 and Tx_D_n = 0x'1F, the symbols corresponding to the ESD_Ext_Err row shall be used.

The symbols corresponding to the ESD1 row in table 40-1 shall be used when the condition (!tx_enable_{n-2}) * (tx_enable_{n-3}) = 1, in the absence of Carrier Extend Error indication at time n.

The symbols corresponding to the ESD2_Ext_0 row in table 40-1 shall be used when the condition (!tx_enable_{n-3}) * (tx_enable_{n-4}) * (!tx_error_n) * (!tx_error_{n-1}) = 1.

The symbols corresponding to the ESD2_Ext_1 row in table 40-1 shall be used when the condition (!tx_enable_{n-3}) * (tx_enable_{n-4}) * (!tx_error_n) * (tx_error_{n-1}) = 1.

The symbols corresponding to the ESD2_Ext_2 row in table 40-1 shall be used when the condition (!tx_enable_{n-3}) * (tx_enable_{n-4}) * (tx_error_n) * (tx_error_{n-1}) = 1, in the absence of Carrier Extend Error indication.

Table 40-1—Bit-to-Symbol Mapping (Even Subsets)

		Sd_n[6:8] = [000]	**Sd_n[6:8] = [010]**	**Sd_n[6:8] = [100]**	**Sd_n[6:8] = [110]**
Condition	**Sd_n[5:0]**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**
Normal	000000	0, 0, 0, 0	0, 0,+1,+1	0,+1,+1, 0	0,+1, 0,+1
Normal	000001	-2, 0, 0, 0	-2, 0,+1,+1	-2,+1,+1, 0	-2,+1, 0,+1
Normal	000010	0,-2, 0, 0	0,-2,+1,+1	0,-1,+1, 0	0,-1, 0,+1
Normal	000011	-2,-2, 0, 0	-2,-2,+1,+1	-2,-1,+1, 0	-2,-1, 0,+1
Normal	000100	0, 0,-2, 0	0, 0,-1,+1	0,+1,-1, 0	0,+1,-2,+1
Normal	000101	-2, 0,-2, 0	-2, 0,-1,+1	-2,+1,-1, 0	-2,+1,-2,+1
Normal	000110	0,-2,-2, 0	0,-2,-1,+1	0,-1,-1, 0	0,-1,-2,+1
Normal	000111	-2,-2,-2, 0	-2,-2,-1,+1	-2,-1,-1, 0	-2,-1,-2,+1
Normal	001000	0, 0, 0,-2	0, 0,+1,-1	0,+1,+1,-2	0,+1, 0,-1
Normal	001001	-2, 0, 0,-2	-2, 0,+1,-1	-2,+1,+1,-2	-2,+1, 0,-1
Normal	001010	0,-2, 0,-2	0,-2,+1,-1	0,-1,+1,-2	0,-1, 0,-1
Normal	001011	-2,-2, 0,-2	-2,-2,+1,-1	-2,-1,+1,-2	-2,-1, 0,-1
Normal	001100	0, 0,-2,-2	0, 0,-1,-1	0,+1,-1,-2	0,+1,-2,-1

Table 40-1—Bit-to-Symbol Mapping (Even Subsets)

		$Sd_n[6:8]$ = [000]	$Sd_n[6:8]$ = [010]	$Sd_n[6:8]$ = [100]	$Sd_n[6:8]$ = [110]
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**
Normal	001101	-2, 0,-2,-2	-2, 0,-1,-1	-2,+1,-1,-2	-2,+1,-2,-1
Normal	001110	0,-2,-2,-2	0,-2,-1,-1	0,-1,-1,-2	0,-1,-2,-1
Normal	001111	-2,-2,-2,-2	-2,-2,-1,-1	-2,-1,-1,-2	-2,-1,-2,-1
Normal	010000	+1,+1,+1,+1	+1,+1, 0, 0	+1, 0, 0,+1	+1, 0,+1, 0
Normal	010001	-1,+1,+1,+1	-1,+1, 0, 0	-1, 0, 0,+1	-1, 0,+1, 0
Normal	010010	+1,-1,+1,+1	+1,-1, 0, 0	+1,-2, 0,+1	+1,-2,+1, 0
Normal	010011	-1,-1,+1,+1	-1,-1, 0, 0	-1,-2, 0,+1	-1,-2,+1, 0
Normal	010100	+1,+1,-1,+1	+1,+1,-2, 0	+1, 0,-2,+1	+1, 0,-1, 0
Normal	010101	-1,+1,-1,+1	-1,+1,-2, 0	-1, 0,-2,+1	-1, 0,-1, 0
Normal	010110	+1,-1,-1,+1	+1,-1,-2, 0	+1,-2,-2,+1	+1,-2,-1, 0
Normal	010111	-1,-1,-1,+1	-1,-1,-2, 0	-1,-2,-2,+1	-1,-2,-1, 0
Normal	011000	+1,+1,+1,-1	+1,+1, 0,-2	+1, 0, 0,-1	+1, 0,+1,-2
Normal	011001	-1,+1,+1,-1	-1,+1, 0,-2	-1, 0, 0,-1	-1, 0,+1,-2
Normal	011010	+1,-1,+1,-1	+1,-1, 0,-2	+1,-2, 0,-1	+1,-2,+1,-2
Normal	011011	-1,-1,+1,-1	-1,-1, 0,-2	-1,-2, 0,-1	-1,-2,+1,-2
Normal	011100	+1,+1,-1,-1	+1,+1,-2,-2	+1, 0,-2,-1	+1, 0,-1,-2
Normal	011101	-1,+1,-1,-1	-1,+1,-2,-2	-1, 0,-2,-1	-1, 0,-1,-2
Normal	011110	+1,-1,-1,-1	+1,-1,-2,-2	+1,-2,-2,-1	+1,-2,-1,-2
Normal	011111	-1,-1,-1,-1	-1,-1,-2,-2	-1,-2,-2,-1	-1,-2,-1,-2
Normal	100000	+2, 0, 0, 0	+2, 0,+1,+1	+2,+1,+1, 0	+2,+1, 0,+1
Normal	100001	+2,-2, 0, 0	+2,-2,+1,+1	+2,-1,+1, 0	+2,-1, 0,+1
Normal	100010	+2, 0,-2, 0	+2, 0,-1,+1	+2,+1,-1, 0	+2,+1,-2,+1
Normal	100011	+2,-2,-2, 0	+2,-2,-1,+1	+2,-1,-1, 0	+2,-1,-2,+1
Normal	100100	+2, 0, 0,-2	+2, 0,+1,-1	+2,+1,+1,-2	+2,+1, 0,-1
Normal	100101	+2,-2, 0,-2	+2,-2,+1,-1	+2,-1,+1,-2	+2,-1, 0,-1
Normal	100110	+2, 0,-2,-2	+2, 0,-1,-1	+2,+1,-1,-2	+2,+1,-2,-1
Normal	100111	+2,-2,-2,-2	+2,-2,-1,-1	+2,-1,-1,-2	+2,-1,-2,-1
Normal	101000	0, 0,+2, 0	+1,+1,+2, 0	+1, 0,+2,+1	0,+1,+2,+1
Normal	101001	-2, 0,+2, 0	-1,+1,+2, 0	-1, 0,+2,+1	-2,+1,+2,+1

Table 40-1—Bit-to-Symbol Mapping (Even Subsets)

		$Sd_n[6:8]$ = [000]	$Sd_n[6:8]$ = [010]	$Sd_n[6:8]$ = [100]	$Sd_n[6:8]$ = [110]
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**
Normal	101010	0,-2,+2, 0	+1,-1,+2, 0	+1,-2,+2,+1	0,-1,+2,+1
Normal	101011	-2,-2,+2, 0	-1,-1,+2, 0	-1,-2,+2,+1	-2,-1,+2,+1
Normal	101100	0, 0,+2,-2	+1,+1,+2,-2	+1, 0,+2,-1	0,+1,+2,-1
Normal	101101	-2, 0,+2,-2	-1,+1,+2,-2	-1, 0,+2,-1	-2,+1,+2,-1
Normal	101110	0,-2,+2,-2	+1,-1,+2,-2	+1,-2,+2,-1	0,-1,+2,-1
Normal	101111	-2,-2,+2,-2	-1,-1,+2,-2	-1,-2,+2,-1	-2,-1,+2,-1
Normal	110000	0,+2, 0, 0	0,+2,+1,+1	+1,+2, 0,+1	+1,+2,+1, 0
Normal	110001	-2,+2, 0, 0	-2,+2,+1,+1	-1,+2, 0,+1	-1,+2,+1, 0
Normal	110010	0,+2,-2, 0	0,+2,-1,+1	+1,+2,-2,+1	+1,+2,-1, 0
Normal	110011	-2,+2,-2, 0	-2,+2,-1,+1	-1,+2,-2,+1	-1,+2,-1, 0
Normal	110100	0,+2, 0,-2	0,+2,+1,-1	+1,+2, 0,-1	+1,+2,+1,-2
Normal	110101	-2,+2, 0,-2	-2,+2,+1,-1	-1,+2, 0,-1	-1,+2,+1,-2
Normal	110110	0,+2,-2,-2	0,+2,-1,-1	+1,+2,-2,-1	+1,+2,-1,-2
Normal	110111	-2,+2,-2,-2	-2,+2,-1,-1	-1,+2,-2,-1	-1,+2,-1,-2
Normal	111000	0, 0, 0,+2	+1,+1, 0,+2	0,+1,+1,+2	+1, 0,+1,+2
Normal	111001	-2, 0, 0,+2	-1,+1, 0,+2	-2,+1,+1,+2	-1, 0,+1,+2
Normal	111010	0,-2, 0,+2	+1,-1, 0,+2	0,-1,+1,+2	+1,-2,+1,+2
Normal	111011	-2,-2, 0,+2	-1,-1, 0,+2	-2,-1,+1,+2	-1,-2,+1,+2
Normal	111100	0, 0,-2,+2	+1,+1,-2,+2	0,+1,-1,+2	+1, 0,-1,+2
Normal	111101	-2, 0,-2,+2	-1,+1,-2,+2	-2,+1,-1,+2	-1, 0,-1,+2
Normal	111110	0,-2,-2,+2	+1,-1,-2,+2	0,-1,-1,+2	+1,-2,-1,+2
Normal	111111	-2,-2,-2,+2	-1,-1,-2,+2	-2,-1,-1,+2	-1,-2,-1,+2
Xmt_Err	XXXXXX	0,+2,+2,0	+1,+1,+2,+2	+2,+1,+1,+2	+2,+1,+2,+1
CSExtend_Err	XXXXXX	-2,+2,+2,-2	-1,-1,+2,+2	+2,-1,-1,+2	+2,-1,+2,-1
CSExtend	XXXXXX	+2, 0, 0,+2	+2,+2,+1,+1	+1,+2,+2,+1	+1,+2,+1,+2
CSReset	XXXXXX	+2,-2,-2,+2	+2,+2,-1,-1	-1,+2,+2,-1	-1,+2,-1,+2
SSD1	XXXXXX	+2,+2,+2,+2	NA	NA	NA
SSD2	XXXXXX	+2,+2,+2,-2	NA	NA	NA
ESD1	XXXXXX	+2,+2,+2,+2	NA	NA	NA

Table 40-1—Bit-to-Symbol Mapping (Even Subsets)

		$Sd_n[6:8]$ = [000]	$Sd_n[6:8]$ = [010]	$Sd_n[6:8]$ = [100]	$Sd_n[6:8]$ = [110]
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**
ESD2_Ext_0	XXXXXX	+2,+2,+2,-2	NA	NA	NA
ESD2_Ext_1	XXXXXX	+2,+2,-2,+2	NA	NA	NA
ESD2_Ext_2	XXXXXX	+2,-2,+2,+2	NA	NA	NA
ESD_Ext_Err	XXXXXX	-2,+2,+2,+2	NA	NA	NA

Table 40-2—Bit-to-Symbol Mapping (Odd Subsets)

		$Sd_n[6:8]$ = [001]	$Sd_n[6:8]$ = [011]	$Sd_n[6:8]$ = [101]	$Sd_n[6:8]$ = [111]
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**
Normal	000000	0, 0, 0,+1	0, 0,+1, 0	0,+1,+1,+1	0,+1, 0, 0
Normal	000001	-2, 0, 0,+1	-2, 0,+1, 0	-2,+1,+1,+1	-2,+1, 0, 0
Normal	000010	0,-2, 0,+1	0,-2,+1, 0	0,-1,+1,+1	0,-1, 0, 0
Normal	000011	-2,-2, 0,+1	-2,-2,+1, 0	-2,-1,+1,+1	-2,-1, 0, 0
Normal	000100	0, 0,-2,+1	0, 0,-1, 0	0,+1,-1,+1	0,+1,-2, 0
Normal	000101	-2, 0,-2,+1	-2, 0,-1, 0	-2,+1,-1,+1	-2,+1,-2, 0
Normal	000110	0,-2,-2,+1	0,-2,-1, 0	0,-1,-1,+1	0,-1,-2, 0
Normal	000111	-2,-2,-2,+1	-2,-2,-1, 0	-2,-1,-1,+1	-2,-1,-2, 0
Normal	001000	0, 0, 0,-1	0, 0,+1,-2	0,+1,+1,-1	0,+1, 0,-2
Normal	001001	-2, 0, 0,-1	-2, 0,+1,-2	-2,+1,+1,-1	-2,+1, 0,-2
Normal	001010	0,-2, 0,-1	0,-2,+1,-2	0,-1,+1,-1	0,-1, 0,-2
Normal	001011	-2,-2, 0,-1	-2,-2,+1,-2	-2,-1,+1,-1	-2,-1, 0,-2
Normal	001100	0, 0,-2,-1	0, 0,-1,-2	0,+1,-1,-1	0,+1,-2,-2
Normal	001101	-2, 0,-2,-1	-2, 0,-1,-2	-2,+1,-1,-1	-2,+1,-2,-2
Normal	001110	0,-2,-2,-1	0,-2,-1,-2	0,-1,-1,-1	0,-1,-2,-2
Normal	001111	-2,-2,-2,-1	-2,-2,-1,-2	-2,-1,-1,-1	-2,-1,-2,-2
Normal	010000	+1,+1,+1, 0	+1,+1, 0,+1	+1, 0, 0, 0	+1, 0,+1,+1
Normal	010001	-1,+1,+1, 0	-1,+1, 0,+1	-1, 0, 0, 0	-1, 0,+1,+1
Normal	010010	+1,-1,+1, 0	+1,-1, 0,+1	+1,-2, 0, 0	+1,-2,+1,+1

Table 40-2—Bit-to-Symbol Mapping (Odd Subsets)

		$Sd_n[6:8]$ = [001]	$Sd_n[6:8]$ = [011]	$Sd_n[6:8]$ = [101]	$Sd_n[6:8]$ = [111]
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**
Normal	010011	-1,-1,+1, 0	-1,-1, 0,+1	-1,-2, 0, 0	-1,-2,+1,+1
Normal	010100	+1,+1,-1, 0	+1,+1,-2,+1	+1, 0,-2, 0	+1, 0,-1,+1
Normal	010101	-1,+1,-1, 0	-1,+1,-2,+1	-1, 0,-2, 0	-1, 0,-1,+1
Normal	010110	+1,-1,-1, 0	+1,-1,-2,+1	+1,-2,-2, 0	+1,-2,-1,+1
Normal	010111	-1,-1,-1, 0	-1,-1,-2,+1	-1,-2,-2, 0	-1,-2,-1,+1
Normal	011000	+1,+1,+1,-2	+1,+1, 0,-1	+1, 0, 0,-2	+1, 0,+1,-1
Normal	011001	-1,+1,+1,-2	-1,+1, 0,-1	-1, 0, 0,-2	-1, 0,+1,-1
Normal	011010	+1,-1,+1,-2	+1,-1, 0,-1	+1,-2, 0,-2	+1,-2,+1,-1
Normal	011011	-1,-1,+1,-2	-1,-1, 0,-1	-1,-2, 0,-2	-1,-2,+1,-1
Normal	011100	+1,+1,-1,-2	+1,+1,-2,-1	+1, 0,-2,-2	+1, 0,-1,-1
Normal	011101	-1,+1,-1,-2	-1,+1,-2,-1	-1, 0,-2,-2	-1, 0,-1,-1
Normal	011110	+1,-1,-1,-2	+1,-1,-2,-1	+1,-2,-2,-2	+1,-2,-1,-1
Normal	011111	-1,-1,-1,-2	-1,-1,-2,-1	-1,-2,-2,-2	-1,-2,-1,-1
Normal	100000	+2, 0, 0,+1	+2, 0,+1, 0	+2,+1,+1,+1	+2,+1, 0, 0
Normal	100001	+2,-2, 0,+1	+2,-2,+1, 0	+2,-1,+1,+1	+2,-1, 0, 0
Normal	100010	+2, 0,-2,+1	+2, 0,-1, 0	+2,+1,-1,+1	+2,+1,-2, 0
Normal	100011	+2,-2,-2,+1	+2,-2,-1, 0	+2,-1,-1,+1	+2,-1,-2, 0
Normal	100100	+2, 0, 0,-1	+2, 0,+1,-2	+2,+1,+1,-1	+2,+1, 0,-2
Normal	100101	+2,-2, 0,-1	+2,-2,+1,-2	+2,-1,+1,-1	+2,-1, 0,-2
Normal	100110	+2, 0,-2,-1	+2, 0,-1,-2	+2,+1,-1,-1	+2,+1,-2,-2
Normal	100111	+2,-2,-2,-1	+2,-2,-1,-2	+2,-1,-1,-1	+2,-1,-2,-2
Normal	101000	0, 0,+2,+1	+1,+1,+2,+1	+1, 0,+2, 0	0,+1,+2, 0
Normal	101001	-2, 0,+2,+1	-1,+1,+2,+1	-1, 0,+2, 0	-2,+1,+2, 0
Normal	101010	0,-2,+2,+1	+1,-1,+2,+1	+1,-2,+2, 0	0,-1,+2, 0
Normal	101011	-2,-2,+2,+1	-1,-1,+2,+1	-1,-2,+2, 0	-2,-1,+2, 0
Normal	101100	0, 0,+2,-1	+1,+1,+2,-1	+1, 0,+2,-2	0,+1,+2,-2
Normal	101101	-2, 0,+2,-1	-1,+1,+2,-1	-1, 0,+2,-2	-2,+1,+2,-2
Normal	101110	0,-2,+2,-1	+1,-1,+2,-1	+1,-2,+2,-2	0,-1,+2,-2
Normal	101111	-2,-2,+2,-1	-1,-1,+2,-1	-1,-2,+2,-2	-2,-1,+2,-2

Table 40-2—Bit-to-Symbol Mapping (Odd Subsets)

		$Sd_n[6:8]$ = [001]	$Sd_n[6:8]$ = [011]	$Sd_n[6:8]$ = [101]	$Sd_n[6:8]$ = [111]
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**
Normal	110000	0,+2, 0,+1	0,+2,+1, 0	+1,+2, 0, 0	+1,+2,+1,+1
Normal	110001	-2,+2, 0,+1	-2,+2,+1, 0	-1,+2, 0, 0	-1,+2,+1,+1
Normal	110010	0,+2,-2,+1	0,+2,-1, 0	+1,+2,-2, 0	+1,+2,-1,+1
Normal	110011	-2,+2,-2,+1	-2,+2,-1, 0	-1,+2,-2, 0	-1,+2,-1,+1
Normal	110100	0,+2, 0,-1	0,+2,+1,-2	+1,+2, 0,-2	+1,+2,+1,-1
Normal	110101	-2,+2, 0,-1	-2,+2,+1,-2	-1,+2, 0,-2	-1,+2,+1,-1
Normal	110110	0,+2,-2,-1	0,+2,-1,-2	+1,+2,-2,-2	+1,+2,-1,-1
Normal	110111	-2,+2,-2,-1	-2,+2,-1,-2	-1,+2,-2,-2	-1,+2,-1,-1
Normal	111000	+1,+1,+1,+2	0, 0,+1,+2	+1, 0, 0,+2	0,+1, 0,+2
Normal	111001	-1,+1,+1,+2	-2, 0,+1,+2	-1, 0, 0,+2	-2,+1, 0,+2
Normal	111010	+1,-1,+1,+2	0,-2,+1,+2	+1,-2, 0,+2	0,-1, 0,+2
Normal	111011	-1,-1,+1,+2	-2,-2,+1,+2	-1,-2, 0,+2	-2,-1, 0,+2
Normal	111100	+1,+1,-1,+2	0, 0,-1,+2	+1, 0,-2,+2	0,+1,-2,+2
Normal	111101	-1,+1,-1,+2	-2, 0,-1,+2	-1, 0,-2,+2	-2,+1,-2,+2
Normal	111110	+1,-1,-1,+2	0,-2,-1,+2	+1,-2,-2,+2	0,-1,-2,+2
Normal	111111	-1,-1,-1,+2	-2,-2,-1,+2	-1,-2,-2,+2	-2,-1,-2,+2
Xmt_Err	XXXXXX	+2,+2, 0,+1	0,+2,+1,+2	+1,+2,+2, 0	+2,+1,+2, 0
CSExtend_Err	XXXXXX	+2,+2, -2,-1	-2,+2,-1,+2	-1,+2,+2,-2	+2,-1,+2,-2
CSExtend	XXXXXX	+2, 0,+2,+1	+2, 0,+1,+2	+1, 0,+2,+2	+2.+1. 0.+2
CSReset	XXXXXX	+2,-2,+2,-1	+2,-2,-1,+2	-1,-2,+2,+2	+2,-1,-2,+2

40.4.1.2.6 Generation of A_n, B_n, C_n, D_n

The four bits $Sg_n[3:0]$ are used to randomize the signs of the quinary symbols (A_n, B_n, C_n, D_n) so that each symbol stream has no DC bias. The bits are used to generate binary symbols (SnA_n, SnB_n, SnC_n, SnD_n) that when multiplied by the quinary symbols (TA_n, TB_n, TC_n, TD_n) result in (A_n, B_n, C_n, D_n).

PCS Transmit ensures a distinction between symbols transmitted during data versus those transmitted during idle by reversing the mapping of the sign bits when the condition (tx_enable_{n-2} + tx_enable_{n-4}) = 1. This sign reversal is controlled by the variable $Srev_n$ defined as

$$Srev_n = tx\_enable_{n-2} + tx\_enable_{n-4}$$

The binary symbols SnA_n, SnB_n, SnC_n and SnD_n are defined using $Sg_n[3:0]$ as follows

$$SnA_n = \begin{cases} +1 \text{ if } (Sg_n[0] \oplus Srev_n = 0) \\ -1 \text{ else} \end{cases}$$

$$SnB_n = \begin{cases} +1 \text{ if } (Sg_n[1] \oplus Srev_n = 0) \\ -1 \text{ else} \end{cases}$$

$$SnC_n = \begin{cases} +1 \text{ if } (Sg_n[2] \oplus Srev_n = 0) \\ -1 \text{ else} \end{cases}$$

$$SnD_n = \begin{cases} +1 \text{ if } (Sg_n[3] \oplus Srev_n = 0) \\ -1 \text{ else} \end{cases}$$

The quinary symbols (A_n, B_n, C_n, D_n) are generated as the product of (SnA_n, SnB_n, SnC_n, SnD_n) and (TA_n, TB_n, TC_n, TD_n) respectively.

$$A_n = TA_n \times SnA_n$$

$$B_n = TB_n \times SnB_n$$

$$C_n = TC_n \times SnC_n$$

$$D_n = TD_n \times SnD_n$$

40.4.1.3 PCS Receive function

The PCS Receive function shall conform to the PCS Receive state diagram in figure figure 40-10.

The PCS Receive function accepts quartets of detected quinary symbols provided by the PMA Receive function via the parameter rx_symb_vector. To achieve correct operation, PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode. PCS Receive generates the sequence of vectors of four quinary symbols (RA_n, RB_n, RC_n, RD_n) and indicates the reliability of receiver operations by setting the parameter loc_rcvr_status to OK, RNOK or TNOK. The sequence (RA_n, RB_n, RC_n, RD_n) is processed to generate the signals RXD<7:0>, RX_DV, and RX_ER, which are presented to the GMII. PCS Receive detects the transmission of a stream of data from the remote station and conveys this information to the PCS Carrier Sense and PCS Collision Presence functions via the parameter receiving.

40.4.1.3.1 Receiver descrambler polynomials

For side-stream descrambling, the master PHY shall employ the receiver descrambler generator polynomial $g'_M(x) = 1 + x^{20} + x^{33}$ and the slave PHY shall employ the receiver descrambler generator polynomial $g'_S(x) = 1 + x^{13} + x^{33}$.

40.4.1.3.2 Decoding of quinary symbols

At the beginning of a stream of data, PCS Receive detects “SSD” and asserts the signal RX_DV. Detection of “SSD” is achieved by processing two consecutive vectors (RA_{n-1}, RB_{n-1}, RC_{n-1}, RD_{n-1}) and (RA_n, RB_n, RC_n and RD_n) at each time n. Upon detection of “SSD”, PCS Receive also assigns the value TRUE to the parameter receiving that is provided to the PCS Carrier Sense and Collision Presence functions.

During reception of a stream of data, PCS Receive checks that the symbols RA_n, RB_n, RC_n, RD_n follow the encoding rule defined in 40.4.1.2 whenever they assume values ± 2. PCS Receive processes two consecutive vectors at each time n to detect “ESD”. Upon detection of “ESD”, PCS Receive de-asserts the signal RX_DV, and assigns the value FALSE to the parameter receiving. If a violation of the encoding rules is detected, PCS Receive asserts the signal RX_ER for at least one symbol period.

40.4.1.4 PCS Carrier Sense function

The PCS Carrier Sense function shall conform to the PCS Carrier Sense state diagram in figure 40-11.

The PCS Carrier Sense function controls the GMII signal CRS according to the rules presented in this clause. While link_status = OK, CRS is asserted whenever receiving=TRUE or tx_enable=1 or tx_error=1.

40.4.1.5 PCS Collision Presence function

A PCS collision is defined as the simultaneous occurrence of tx_enable=1 or tx_error=1 and the assertion of the parameter receiving=TRUE while link_status=OK. While a PCS collision is detected, the GMII signal COL shall be asserted. At other times COL shall remain de-asserted.

40.4.2 PCS interfaces

40.4.2.1 PCS - GMII interface signals

The following signals are formally defined in 35.2.2. Jabber detection as specified in 22.2.4.2.12 is not required by this specification

Table 40-3— GMII interface signals

Signal name	Meaning
GTX_CLK	Transmit Clock
TXD<7:0>	Transmit Data
TX_ER	Indicates Transmit Error/ Carrier Extension
TX_EN	Frames Transmit Data
COL	Collision Indication
CRS	Non-Idle Medium Indication
RX_CLK	Receive Clock
RXD<7:0>	Receive Data
RX_DV	Frames Receive SFD and DATA

Table 40-3— GMII interface signals

Signal name	Meaning
RX_ER	Receive Error Indication/ Carrier Extension
MDC	Management Data Clock
MDIO	Management Data

40.4.2.2 PCS - management entity signals

The management interface has pervasive connections to all functions. Operation of the management control lines MDC and MDIO, and requirements for managed objects inside the PCS and PMA, are specified in clauses 22 and 30, respectively.

No spurious signals shall be emitted onto the MDI when the PHY is held in power down mode as defined in 22.2.4.1.5, independently of the value of TX_EN, or when released from power down mode, or when external power is first applied to the PHY.

40.4.3 Frame structure

Frames passed from the PCS to the PMA sublayer shall have the structure shown in figure 40-7. This figure shows the temporal relationship between the signals tx_enable_n, and TXD[7:0] and the sequences of quinary symbol quartets (A_n, B_n, C_n, D_n) in correspondence of transitions from the idle mode to transmission of data and vice versa. Time proceeds from left to right in the figure.

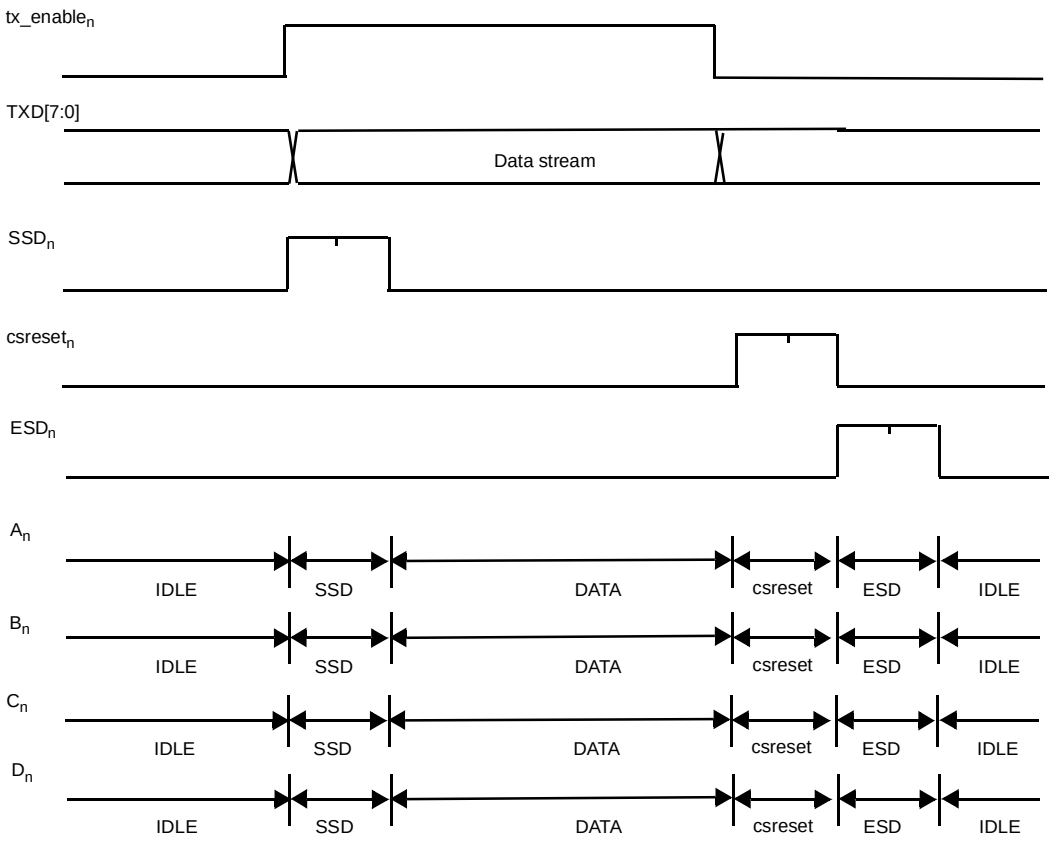


Figure 40-7—PCS sublayer to PMA sublayer frame structure

40.4.4 State variables

40.4.4.1 Variables

CEXT

A sequence of vectors of four quinary symbols generated in idle mode to denote Carrier Extension, as specified in 40.4.1.2.

CEXT_Err

A sequence of vectors of four quinary symbols generated in idle mode to denote Carrier Extension with error indication, as specified in 40.4.1.2.

COL

The COL signal of the GMII as specified in clause 35.

config

The config parameter set by PHY Control and passed to the PCS via the PHYC_CONFIG.indicate primitive.

Values: MASTER and SLAVE.

CRS

The CRS signal of the GMII as specified in clause 35.

CSExtend

A vector of four quinary symbols corresponding to convolutional encoder reset condition during carrier extension, as specified in 40.4.1.2.

CSExtend_Err

A vector of four quinary symbols corresponding to convolutional encoder reset condition during carrier extension with error indication, as specified in 40.4.1.2.

CSReset

A vector of four quinary symbols corresponding to convolutional encoder reset condition in the absence of carrier extension, as specified in 40.4.1.2.

DATA

A sequence of vectors of four quinary symbols corresponding to valid data, as specified in 40.4.1.2.

ESD1

A vector of four quinary symbols corresponding to the first byte of End-of-Stream delimiter, as specified in 40.4.1.2.

ESD2_Ext_0

A vector of four quinary symbols corresponding to the second byte of End-of-Stream delimiter in the absence of carrier extension over the two ESD bytes, as specified in 40.4.1.2.

ESD2_Ext_1

A vector of four quinary symbols corresponding to the second byte of End-of-Stream delimiter when carrier extension is indicated during the first byte of the End-of-Stream delimiter, but not during the second byte, as specified in 40.4.1.2.

ESD2_Ext_2

A vector of four quinary symbols corresponding to the second byte of End-of-Stream delimiter when carrier extension is indicated during the two bytes of the End-of-Stream delimiter, as specified in 40.4.1.2.

ESD_Ext_Err

A vector of four quinary symbols corresponding to either the first or second byte of End-of-Stream delimiter when carrier extension with error is indicated during the End-of-Stream delimiter, as specified in 40.4.1.2.

IDLE

A sequence of vectors of four quinary symbols generated in idle mode in the absence of carrier extension or carrier extension with error indication, as specified in 40.4.1.2.

link_status

The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indicate primitive.

Values: OK, READY, and FAIL

loc_rcvr_status

The loc_rcvr_status parameter generated by PCS Receive.

Values: OK, RNOK and TNOK

pcs_reset

The pcs_reset parameter set by the PCS Reset function.

Values: ON and OFF

(RA_n, RB_n, RC_n, RD_n)

The vector of the four correctly aligned most recently received quinary symbols generated by PCS Receive.

receiving

The receiving parameter generated by the PCS Receive function.

Values: TRUE and FALSE

rem_rcvr_status

The rem_rcvr_status parameter generated by PCS Receive.

Values: OK and NOT_OK

Rx_n

Alias for (RA_n, RB_n, RC_n, RD_n).

rxerror_status

The rxerror_status parameter set by the PCS Receive function. Although this variable is set by PCS Receive, it achieves the same function as the variable rxerror_status of clause 24 that is set by PMA and communicated through the PMA_RXERROR.indicate primitive.

Values: ERROR and NO_ERROR

RX_DV

The RX_DV signal of the GMII as specified in clause 35.

RX_ER

The RX_ER signal of the GMII as specified in clause 35.

rx_symb_vector

A vector of four quinary symbols received by the PMA and passed to the PCS via the PMA_UNITDATA.indicate primitive.

Value: SYMB_QUARTET

RXD[7:0]

The RXD<7:0> signal of the GMII as specified in clause 35.

SSD

Two consecutive vectors of four quinary symbols corresponding to the Start-of-Stream delimiter, as specified in 40.4.1.2.

tx_enable

The tx_enable parameter generated by PCS Transmit as specified in 40.4.1.2.

tx_error

The tx_error parameter generated by PCS Transmit as specified in 40.4.1.2.

TX_ER
The TX_ER signal of the GMII as specified in clause 35.

tx_mode
The tx_mode parameter set by PHY Control and passed to the PCS via the PHYC_TXMODE.indicate primitive.

Values: SEND_Z, SEND_N and SEND_I

tx_symb_vector
A vector of four quinary symbols generated by the PCS Transmit function and passed to the PMA via the PMA_UNITDATA.request primitive.

Value: SYMB_QUARTET

Xmt_Err
A vector of four quinary symbols corresponding to a transmit error indication during normal data transmission, as specified in 40.4.1.2.

40.4.4.2 Timer

symb_timer

A continuous free-running timer. The condition symb_timer_done becomes true upon timer expiration.

Restart time: Immediately after expiration; timer restart resets the condition symb_timer_done.

Duration: 8 ns nominal.

TX_CLK shall be generated synchronously with symb_timer (see tolerance required for TX_CLK in 40.6.1.2.6). In the PCS Transmit state diagram, the message PMA_UNITDATA.request is issued concurrently with symb_timer_done.

40.4.4.3 Messages

PMA_UNITDATA.indicate (rx_symb_vector)
A signal sent by PMA Receive indicating that a vector of four quinary symbols is available in rx_symb_vector.

PMA_UNITDATA.request (tx_symb_vector)
A signal sent to PMA Transmit indicating that a vector of four quinary symbols is available in tx_symb_vector.

PUDI
Alias for PMA_UNITDATA.indicate (rx_symb_vector).

40.4.4.4 Functions

check_end
A function used by the PCS Receive process to detect the reception of valid ESD symbols. The check_end function operates on the next two rx_symb_vectors, (Rx_{n+1}) and (Rx_{n+2}), available via

PMA_UNITDATA.indicate, and returns a Boolean value indicating whether these two consecutive vectors contain symbols corresponding to a valid End-of-Stream Delimiter encoding or not, as specified in 40.4.1.2 and figure 40-9.

Values: TRUE and FALSE

check_idle

A function used by the PCS Receive process to detect the reception of valid idle symbols after an error condition during the process. The check_idle function operates on the current rx_symb_vector and the next three rx_symb_vectors available via PMA_UNITDATA.indicate and returns a Boolean value indicating whether the four consecutive vectors contain symbols corresponding to the IDLE mode encoding or not, as specified in 40.4.1.2.

Values: TRUE and FALSE

40.4.5 State diagrams

40.4.5.1 PCS Data Transmission Enable

The PCS Data Transmission Enabling process generates the signals tx_enable and tx_error, which the PCS Transmit process uses for data and carrier extension encoding. The process uses logical operations on tx_mode, Tx_ER and Tx_EN. The PCS shall implement the Data Transmission Enabling process as depicted in figure 40-8 including compliance with the associated state variables as specified in 40.4.4.

40.4.5.2 PCS Transmit

PCS Transmit sends vectors of four quinary symbols to the PMA via the tx_symb_vector parameter. In normal mode of operation, between streams indicated by the parameter tx_enable, PCS Transmit generates sequences of vectors using the encoding rules defined for the idle mode. Upon assertion of tx_enable, PCS Transmit passes an “SSD” of two consecutive vectors of four quinary symbols to the PMA replacing the preamble bits of a stream of data during these two symbol periods. Following the “SSD”, each TXD<7:0> byte is encoded into a vector of four quinary symbols until tx_enable is de-asserted. If, while tx_enable is asserted, the TX_ER signal is also asserted, PCS Transmit passes to the PMA vectors indicating a transmit error. Note that if the signal TX_ER is asserted while “SSD” is being sent, the transmission of the error condition is delayed until transmission of “SSD” has been completed. Following the de-assertion of tx_enable, a “CsReset” of two consecutive vectors of four quinary symbols, followed by an “ESD” of two consecutive vectors of four quinary symbols is generated, after which the transmission of a sequence indicating the idle mode is resumed. See Section 40.4.1.2 and figure 40-9 for details.

Collision detection is implemented by noting the occurrence of carrier receptions during transmissions, following the model of 10BASE-T. The PCS shall implement the Transmit process as depicted in figure 40-9 including compliance with the associated state variables as specified in 40.4.4.

40.4.5.3 PCS Receive

PCS Receive accepts vectors of four quinary symbols from the PMA via the rx_symb_vector parameter. After correct receiver operation has been achieved, the loc_rcvr_status parameter assumes the value OK, and PCS Receive continuously checks that the received sequence satisfies the encoding rule used in idle mode. As soon as a violation is detected, PCS Receive asserts the parameter receiving and determines whether the violation is due to reception of “SSD” or to a receiver error by examining the last two received vectors (RA_{n-1}, RB_{n-1}, RC_{n-1}, RD_{n-1}) and (RA_n, RB_n, RC_n, RD_n). In the first case, during the two symbol

periods corresponding to “SSD”, PCS Receive replaces “SSD” by preamble bits. Following “SSD”, the signal RX_DV is asserted and each received vector is decoded into a data byte RXD<7:0> until “ESD” is detected. De-assertion of RX_DV and transition to the IDLE state take place upon detection of “ESD”. The signal RX_ER is asserted if a receiver error occurs before proper stream termination. In the second case, the signal RX_ER is asserted and the parameter rxerror_status assumes the value ERROR. De-assertion of RX_DV and transition to the IDLE state (rxerror_status=NO_ERROR) takes place upon detection of four consecutive vectors satisfying the encoding rule used in idle mode.

A premature stream termination is caused by the detection invalid symbols during the reception of a data stream. Then, PCS receive waits for the reception of four consecutive vectors satisfying the encoding rule used in idle mode prior to deasserting the error indication. Note that RX_DV remains asserted during the symbol periods corresponding to the first three idle vectors, while RX_ER=TRUE is signaled on the GMII. The signal RX_ER is also asserted in the LINK FAILED state, which ensures that RX_ER remains asserted for at least one symbol period. The PCS shall implement the Receive process as depicted in figure 40-10, including compliance with the associated state variables as specified in 40.4.4.

The parameters receiving and rxerror_status are communicated to the PCS’s clients by the following primitives:

PCS_CARRIER.indicate (receiving)

A signal generated by PCS Receive to indicate reception of non-idle quinary symbols. The purpose of this primitive is to give clients indication of activity on the underlying continuous-signaling channel.

PCS_RXERROR.indicate (rxerror_status)

A signal generated by PCS Receive to indicate a reception of non-idle/carrier extension symbols that does not start with “SSD”.

40.4.5.4 PCS Carrier Sense

The PCS Carrier Sense process generates the signal CRS on the GMII, which the MAC uses via the Reconciliation sublayer for frame receptions and for deferral. The process operates by performing logical operations on tx_error, tx_enable and receiving. The PCS shall implement the Carrier Sense process as depicted in figure 40-11 including compliance with the associated state variables as specified in 40.4.4.

40.4.6 PCS electrical specifications

The interface between PCS, PMA and PHY Control is an abstract message-passing interface, having no specified electrical properties. Electrical characteristics of the signals passing between the PCS and GMII may be found in clause 35.

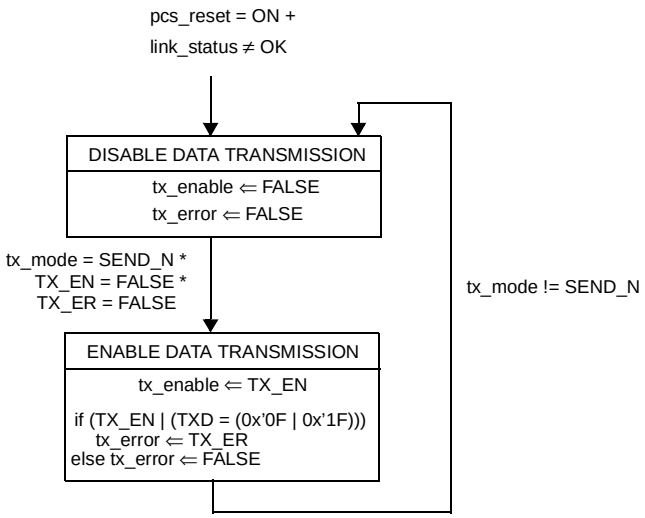
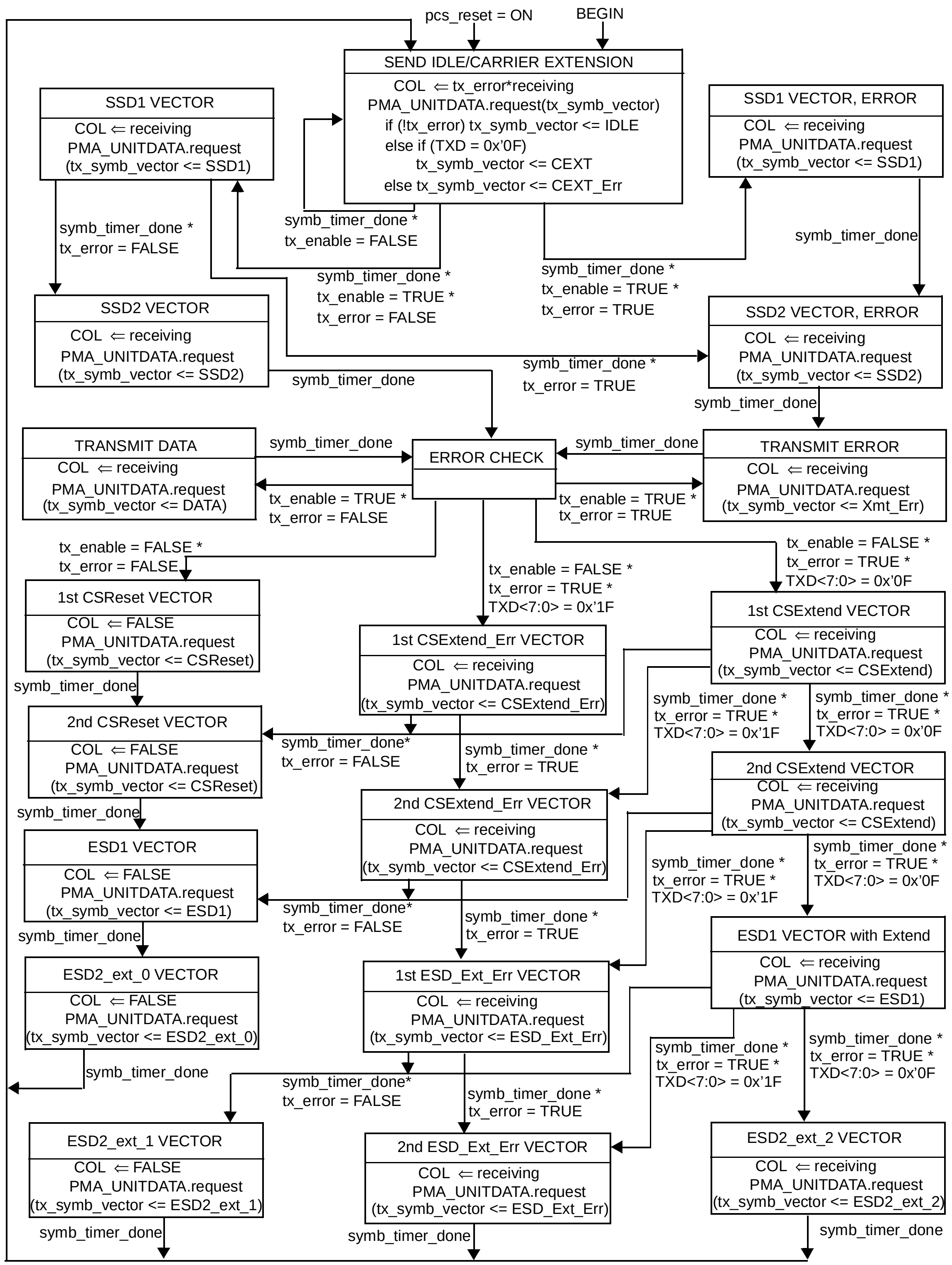


Figure 40-8—PCS Data Transmission Enabling state diagram



Note: The generation of PMA_UNITDATA.request(tx_symb_vector) depends on the parameters config, tx_mode, coding_enable, and loc_rcvr_status as defined in 40.4.1.2 and is not shown explicitly in the state diagram.

Figure 40-9—PCS Transmit State Diagram

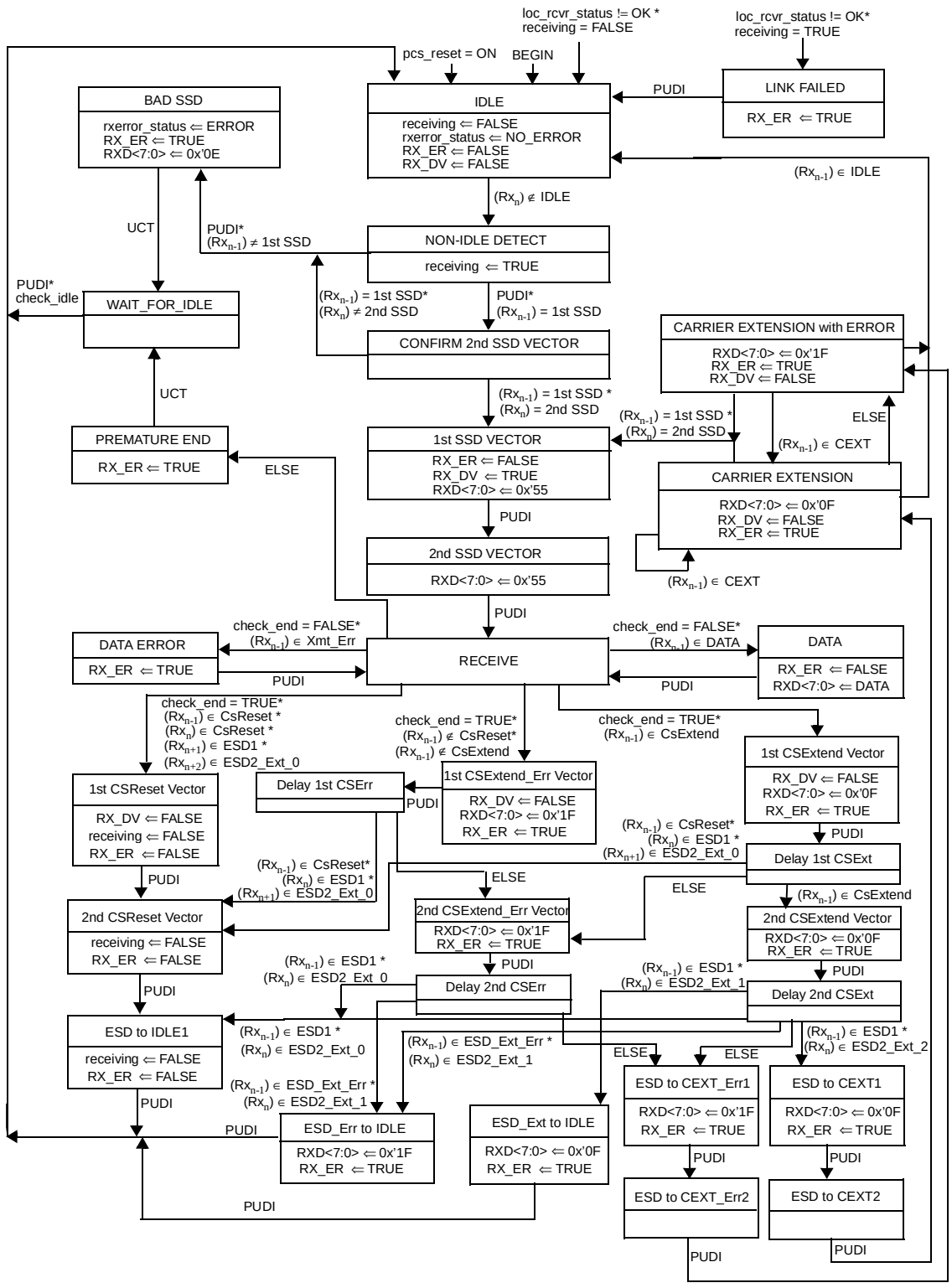


Figure 40-10—PCS Receive State Diagram

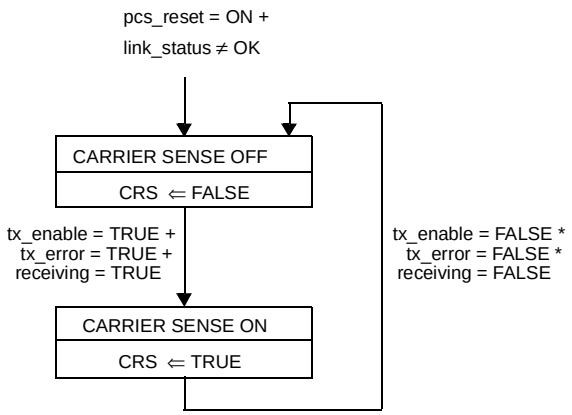


Figure 40-11—PCS Carrier Sense State Diagram

.

40.5 PMA functional specifications and service interface

EDITOR'S NOTE: This clause may change significantly depending on how the PCS and PHY control sections are written.--JLC

40.5.1 PMA functional specifications

The PMA couples messages from a PMA service interface specified in 40.5.2 to the 1000BASE-T baseband medium, specified in 40.8.

The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), specified in 40.9.

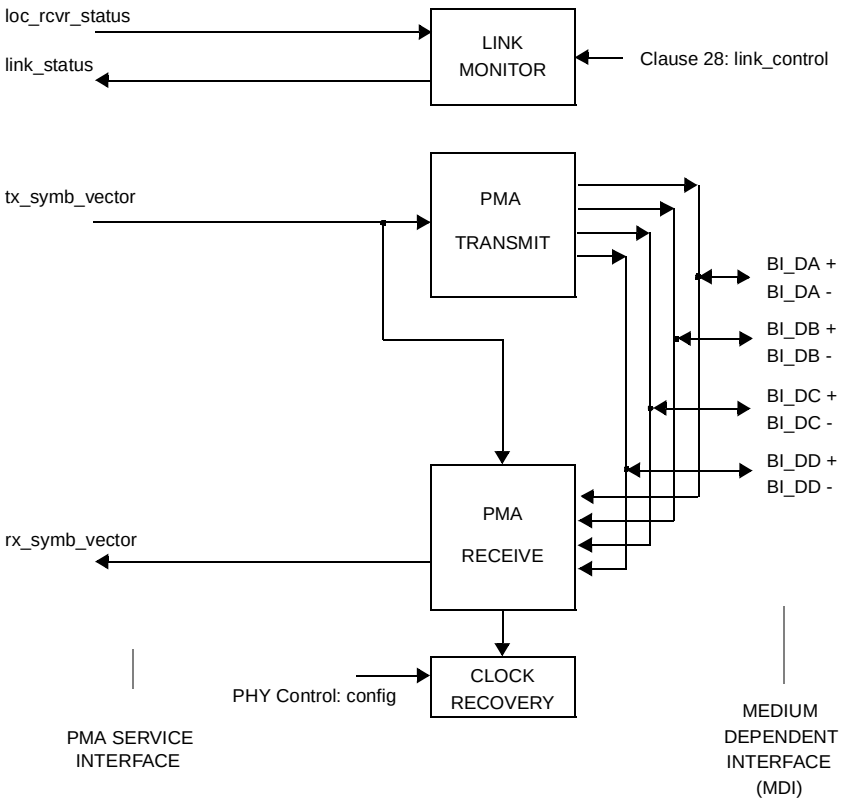


Figure 40-12—PMA reference diagram

40.5.1.1 PMA functions

The PMA sublayer comprises one PMA Reset function and four simultaneous and asynchronous operating functions. The PMA operating functions are PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function. The Reset function may be shared between PMA and PCS sublayers.

The PMA reference diagram, figure 40-12, shows how the operating functions relate to the messages of the PMA Service interface, PHY Control Service interface, and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive, and are not shown in figure 40-12. The management interface and its functions are specified in clause 22.

40.5.1.1.1 PMA Reset function

The PMA Reset function shall be executed any time either of two conditions occur. These two conditions are "power on" and the receipt of a reset request from the management entity. The PMA Reset function initializes all PMA functions and forces Auto-Negotiation to be executed. The PMA Reset function sets pma_reset = ON for the duration of its reset function. All state diagrams take the open ended pma_reset branch upon execution of the PMA Reset function. The reference diagrams do not explicitly show the PMA Reset function.

40.5.1.1.2 PMA Transmit function

The PMA Transmit function comprises four synchronous transmitters to generate four five-level pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC and BI_DD. PMA Transmit shall continuously transmit onto the MDI pulses modulated by the quinary symbols given by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC] and tx_symb_vector[BI_DD], respectively. The four transmitters shall be driven by the same transmit clock. The signals generated by PMA Transmit will follow the mathematical description given in 40.5.1.2.1, and shall comply with the electrical specifications given in 40.7.

40.5.1.1.3 PMA Receive function

The PMA Receive function comprises four independent receivers for quinary pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC and BI_DD. PMA Receive contains the circuits necessary to detect quinary symbol sequences from the signals received at the MDI over receive pairs BI_DA, BI_DB, BI_DC and BI_DD and present these sequences to the PCS Receive function. The signals received at the MDI are described mathematically in 40.5.1.2.2. The PHY shall translate the signals received on pairs BI_DA, BI_DB, BI_DC and BI_DB into the PMA_UNITDATA.indicate parameter rx_symb_vector with a symbol error rate of less than one part in 10^{10}.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization, echo and crosstalk cancellation. The sequence of quinary transmitted symbols tx_symb_vector is needed to perform echo and self near-end crosstalk cancellation.

40.5.1.1.4 Link Monitor function

Link Monitor determines the status of the underlying receive channel. Failure of the underlying receive channel typically causes the PMA's clients to suspend normal operation.

The Auto-Negotiation process notifies Link Monitor whether the device connected to the far end is of type 1000BASE-T. Based on this and other information, Link Monitor sets two important internal variables:

a) the pma_type variable that indicates whether the remote station is of type 1000BASE-T or not,
b) the link_status variable that is sent across the PMA Service interface.

The Link Monitor function shall comply with the state diagram of figure 40-13.

Upon power-on, reset, or release from power-down, the Auto-Negotiation algorithm sets link_control=SCAN_FOR_CARRIER and sends during this period fast link pulses to signal its presence to a remote station. If the presence of a remote station is sensed through reception of fast link pulses, the Auto-Negotiation algorithm sets link_control=DISABLE and exchanges Auto-Negotiation information with the remote station. During this period, link_status=FAIL is asserted. If the presence of a remote 1000BASE-T station is established, the Auto-Negotiation algorithm permits full operation by setting

link_control=ENABLE. As soon as reliable transmission is achieved, the variable link_status=OK is asserted, upon which further PHY operations can take place.

40.5.1.1.5 Clock Recovery function

The Clock Recovery function couples to all four receive pairs. It may provide independent clock phases for sampling the signals on each of the four pairs.

The Clock Recovery function shall provide clocks suitable for signal sampling on each line so that the symbol-error rate indicated in 40.5.1.1.3 is achieved. The received clock signal must be stable and ready for use when training has been completed (loc_rcvr_status=OK).

40.5.1.2 PMA interface messages

The messages between the PMA, PCS, and PHY Control are defined in 40.5.2, PMA Service Interface. Communication through the MDI is summarized below.

40.5.1.2.1 MDI signals transmitted by the PHY

The quinary symbols to be transmitted by the PMA on the four pairs BI_DA, BI_DB, BI_DC and BI_DD are denoted by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC] and tx_symb_vector[BI_DD], respectively. Five-level Pulse Amplitude Modulation over each pair is the modulation scheme employed in 1000BASE-T. It is the function of PMA Transmit to generate on each pair a pulse-amplitude modulated signal of the form

$$s(t) = \sum_k a_k h_1(t - kT)$$

where a_k represents the quinary symbol from the set {-2, -1, 0, +1, +2} to be transmitted at time kT, and $h_1(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 40.7.

40.5.1.2.2 Signals received at the MDI

Signals received at the MDI can be expressed for each pair as pulse-amplitude modulated signals that are corrupted by noise:

$$r(t) = \sum_k a_k h_2(t - kT) + w(t)$$

In this equation, $h_2(t)$ denotes the impulse response of the overall channel from the transmit side up to the MDI at the receive side, and $w(t)$ is a term that includes the contribution of various noise sources. The four signals received on pair BI_DA, BI_DB, BI_DC and BI_DD shall be processed within the PMA Receive function to yield the quinary received symbols rx_symb_vector[BI_DA], rx_symb_vector[BI_DB], rx_symb_vector[BI_DC] and rx_symb_vector[BI_DD].

40.5.1.3 PMA state diagram

40.5.1.3.1 State diagram variables

link_control

The link_control parameter as communicated by the PMA_LINK.request primitive.

Values: See 40.5.2.4.

link_status

The link_status parameter as communicated by the Link Monitor function through the PMA_LINK.indicate primitive.

Values: See 40.5.2.5.

loc_rcvr_status

The loc_rcvr_status parameter as communicated by the PMA_RXSTATUS.request primitive.

Values: See 40.3.2.4.

pma_reset

Allows reset of all PMA functions.

Values: ON and OFF

Set by: PMA Reset

40.5.1.3.2 Timers

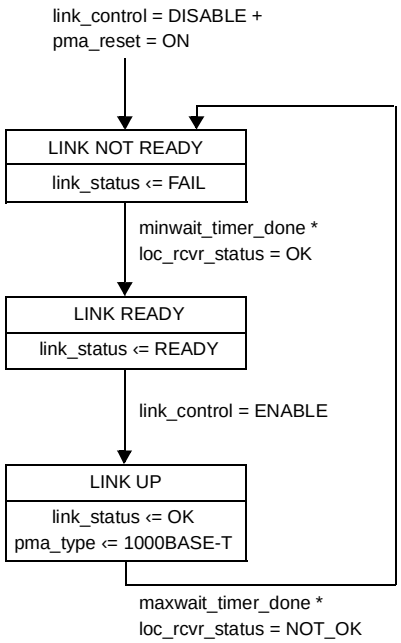
maxwait_timer

Values: See 40.3.4.

minwait_timer

Values: See 40.3.4.

40.5.1.3.3 Link Monitor state diagram



NOTE—The variables link_control and link_status are designated as link_control_1000BASE-T and link_status_1000BASE-T, respectively, by the Auto-Negotiation Arbitration state diagram (figure 28-16)

Figure 40-13—Link Monitor state diagram

40.5.2 PMA service interface

This clause specifies the services provided by the PMA. These services are described in an abstract manner and do not imply any particular implementation. The PMA Service Interface supports the exchange of symbol vectors, status indications, and control signals between the PMA, the PCS and PHY Control. The following primitives are defined:

PMA_TYPE.indicate

PMA_UNITDATA.request

PMA_UNITDATA.indicate

PMA_LINK.request

PMA_LINK.indicate

PMA_CARRIER.indicate

PMA_RXERROR.indicate

The parameter config is passed from PHY Control to the PMA via the primitive PHYC_CONFIG.indicate. The definition of this parameter is given for the PHY Control Service interface in 40.3.2.1 and is not repeated here for the PMA Service interface.

40.5.2.1 PMA_TYPE.indicate

This primitive is generated by the PMA to indicate the nature of the PMA instantiation. Its purpose is to allow clients to support connections to the various types of 100BASE-T and 1000BASE-T PMA entities in a generalized manner.

40.5.2.1.1 Semantics of the primitive

PMA_TYPE.indicate (pma_type)

The pma_type parameter for use with the 1000BASE-T PMA is 1000BASE-T.

40.5.2.1.2 When generated

The PMA shall continuously generate this primitive to indicate the value of pma_type.

40.5.2.1.3 Effect of receipt

The client uses the value of pma_type to define the semantics of the primitives defined at the PMA service interface.

40.5.2.2 PMA_UNITDATA.request

This primitive defines the transfer of quartets of quinary symbols in the form of the tx_symb_vector parameter from the PCS to the PMA. The quinary symbols are obtained in the PCS Transmit function using the encoding rules defined in 40.4.1.2 to represent MII data streams, an idle mode, or other sequences.

40.5.2.2.1 Semantics of the primitive

PMA_UNITDATA.request (tx_symb_vector)

During transmission using 1000BASE-T signaling, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over each of the four transmit pairs BI_DA, BI_DB, BI_DC and BI_DD. The tx_symb_vector parameter takes on the form:

SYMB_4D	A vector of four quinary symbols, one for each of the four transmit pairs BI_DA, BI_DB, BI_DC and BI_DD. Each quinary symbol may take on one of the values -2, -1, 0, +1 or +2.

The quinary symbols that are elements of tx_symb_vector are called, according to the pair on which each will be transmitted, tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD].

40.5.2.2.2 When generated

The PCS generates PMA_UNITDATA.request (SYMB_4D) synchronously with every transmit clock cycle.

40.5.2.2.3 Effect of receipt

Upon receipt of this primitive, the PMA transmits on the MDI the signals corresponding to the indicated quinary symbols. The parameter tx_symb_vector is also used by the PMA Receive function to process the signals received on pairs BI_DA, BI_DB, BI_DC and BI_DD.

40.5.2.3 PMA_UNITDATA.indicate

This primitive defines the transfer of quartets of quinary symbols in the form of the rx_symb_vector parameter from the PMA to the PCS.

40.5.2.3.1 Semantics of the primitive

PMA_UNITDATA.indicate (rx_symb_vector)

During reception of signals using 1000BASE-T signaling, the PMA_UNITDATA.indicate simultaneously conveys to the PCS via the parameter rx_symb_vector the values of the symbols detected on each of the four receive pairs BI_DA, BI_DB, BI_DC and BI_DD. The rx_symbol_vector parameter takes on the form:

SYMB_4D	A vector of four quinary symbols, one for each of the four receive pairs BI_DA, BI_DB, BI_DC and BI_DD. Each quinary symbol may take on one of the values -2, -1, 0, +1 or +2.

The quinary symbols that are elements of rx_symb_vector are called, according to the pair upon which each symbol was received, rx_symbol_vector[BI_DA], rx_symbol_vector[BI_DB], rx_symbol_vector[BI_DC] and rx_symb_vector[BI_DD].

40.5.2.3.2 When generated

The PMA generates PMA_UNITDATA.indicate (SYMB_4D) messages synchronously with signals received at the MDI.

40.5.2.3.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

40.5.2.4 PMA_LINK.request

This primitive allows the Auto-Negotiation algorithm to enable and disable operation of the PMA.

40.5.2.4.1 Semantics of the primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

SCAN_FOR_CARRIER	Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PMA reports link_status=FAIL. PHY processes are disabled.
DISABLE	Set by the Auto-Negotiation algorithm in the event fast link pulses are

	detected. PHY processes are disabled. This allows the Auto-Negotiation algorithm to determine how to configure the link.
ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions.

40.5.2.4.2 When generated

Upon power on, reset, or release from power down, the Auto-Negotiation algorithm issues the message PMA_LINK.request (SCAN_FOR_CARRIER).

40.5.2.4.3 Effect of receipt

While link_control=SCAN_FOR_CARRIER or link_control=DISABLE, the PMA shall report link_status=FAIL. While link_control=ENABLE, PHY Control determines the operations to be performed by the PHY.

40.5.2.5 PMA_LINK.indicate

This primitive is generated by the PMA to indicate the status of the underlying medium. This primitive informs the PCS, PHY Control and the Auto-Negotiation algorithm about the status of the underlying link.

40.5.2.5.1 Semantics of the primitive

PMA_LINK.indicate (link_status)

The link_status parameter can take on one of three values: FAIL, READY, or OK.

FAIL	No valid link established.
READY	Training completed after Auto-Negotiation.
OK	The Link Monitor function indicates that a valid 1000BASE-T link is established. Reliable reception of signals transmitted from the remote PHY is possible.

40.5.2.5.2 When generated

The PMA shall generate this primitive to indicate the value of link_status in compliance with the state diagrams given in figure 40-13.

40.5.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 40.4.4.1 and <TBD Reference to PHY Control>.

40.5.2.6 PMA_CARRIER.indicate

This primitive is identical to PCS_CARRIER.indicate defined in 40.4.1.4. It is not explicitly shown in the PMA reference diagram.

40.5.2.7 PMA_RXERROR.indicate

This primitive is identical to PCS_RXERROR.indicate defined in 40.4.4.1. It is not explicitly shown in the PMA reference diagram.

40.5.2.8 PMA_RXSTATUS.request

This primitive allows the Link Monitor to determine via the parameter loc_rcvr_status generated by the PCS Receive function whether reliable receiver operations are established. The parameter loc_rcvr_status is also passed from the PCS Receive function to the PHY Control Service interface via the primitive PHYC_RXSTATUS.request. The definition of this parameter is given for the PHY Control Service interface in 40.3.2 and is not repeated here for the PMA Service interface.

40.6 Management functions

1000BASE-T makes extensive use of the management functions provided by the Gigabit Media Independent Interface (clause 35) and the communication and self-configuration functions provided by Auto-Negotiation (clause 28.)

In addition to the provision of MII registers 0, 1, 4, 5, 6, 7, and 8, implementations which support 1000BASE-T shall also provide equivalents to MII registers 9 and 10 (clause 22). Register 9 is used to provide the 1000BASE-T Control Register and register 10 is used to provide the 1000BASE-T Status Register (see figure 40-14.) These registers are used to configure PHYs for testing, to manually configure PHYs for MASTER-SLAVE negotiation, to store the contents of next pages during the Auto-Negotiation process, and to store information reporting the results of the master/slave configuration process as described in the next section.

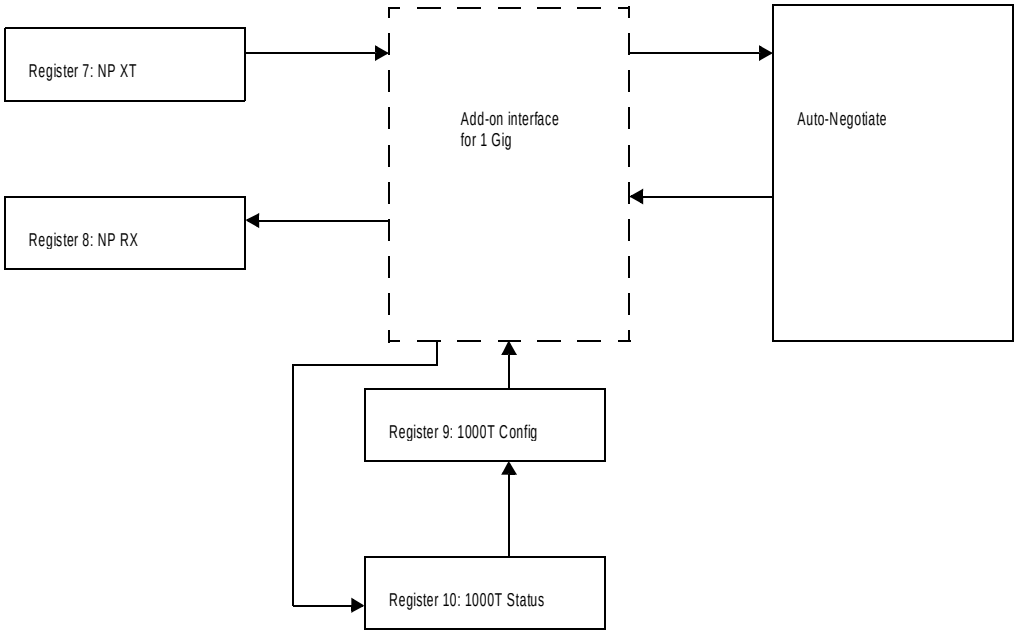


Figure 40-14—1000BASE-T Management Overview

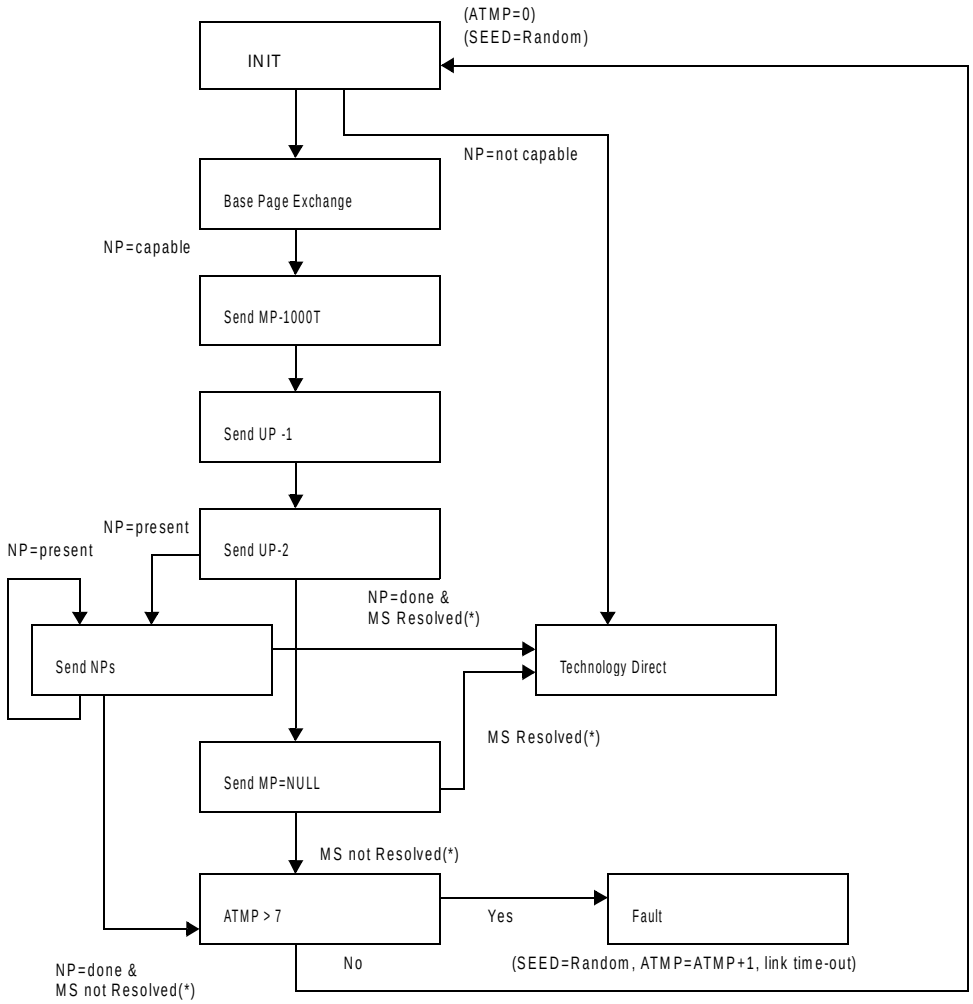
40.6.1 Support for Auto-Negotiation

Support for Auto-Negotiation (clause 28) is a requirement for all 1000BASE-T PHYs. Auto-Negotiation is performed as part of the initial set-up of the link, and allows the PHYs at each end to advertise their capabilities (speed, PHY type, half or full duplex) and to automatically select the operating mode for communication on the link. Auto-negotiation signaling is used for two primary purposes for 1000BASE-T, to negotiate that the PHY is capable of supporting 1000BASE-T half duplex or full duplex transmission, and to determine the master-slave relationship between the PHYs at each end of the link. This relationship is necessary for establishing the timing control of each PHY. The 1000BASE-T master PHY is clocked off of a crystal; the slave PHY uses loop timing where the clock is recovered from the transmitted data stream.

40.6.1.1 1000BASE-T use of Auto-Negotiation and GMII registers 7, 8, 9 and 10

On power-up, before Auto-Negotiation starts, the Auto-Negotiation advertisement register shall have the following configuration: The Selector Field (4.4:0) is set to the appropriate code as specified in Annex 28A. The Acknowledge bit (4:14) is set to logical zero. The Technology Ability Field (4.9:5) is set based on the values set in the GMII Status Register (1.15:11) or equivalent and (4.11:10) is set based on the values set in the GMII Status Register (1.10:9) or equivalent.

When Auto-Negotiation begins, 1000BASE-T implementations sends an Auto-Negotiation base page with bit d15 set to logical one to indicate that a next page follows (see 28.2.1.2, figure 40-15.)



*all next pages from link partner have also been received
*MS Resolved only matters if HCD is 1000T, otherwise bit should be set to true
ATMP = number of MS resolution attempts
SEED = random seen used for MS resolution
MS = Master/Slave
NP = Next Pages
UP = Unformatted Page
MP = Message Page

Figure 40-15—1000BASE-T Next Page Flow

The base page 12shall be followed by a formatted next page containing the 1000BASE-T Technology Ability Message Code (9) which indicates that two unformatted next pages containing the 1000BASE-T Technology Ability fields follow (see table 28C-1.)

Two unformatted next pages shall be sent using the 1000BASE-T Technology Ability fields shown in table 40-8. Register 8 will be used to store the transmitted information while it is being processed as described below.

Editor's Note: Use virtual/shadow registers 7,8 so that it doesn't interfere with normal NP exchange?--MF

Bit U0 through U6 of page 1 shall be copied from MII Register 9.12:6.

Bits U0-U10 of Page 2 shall be used to define the seed used for the MASTER-SLAVE negotiation process described below.

Using the information described above, the PHY performs a MASTER_SLAVE configuration process as defined in 40.6.4.4. This process is conducted at the entrance to the FLP LINK GOOD CHECK state shown in the Auto-Negotiation Arbitration State Diagram (figure 28-16.)

If the local device detects that both the local device and the remote device are of the same type (either repeater or DTE) and that both have generated the same random seek, it generates and transmits a new random seed for MASTER-SLAVE negotiation by restarting the Auto-Negotiation process.

The MASTER-SLAVE configuration process returns one of the three following outcomes:

Successful: Bit 10:15 of the 1000BASE-T Status Register is set to logical zero and bit 10:14 is set to logical one. 1000BASE-T returns control to Auto_Negotiation (at the entrance to the FLP LINK GOOD CHECK state in figure 28-16) and passes the value of MASTER or SLAVE to PHYC_CONFIG.indicate (see 40.3.2.1)

Unsuccessful: link_status_1000BASE-T is set to FAIL and Auto-Negotiation restarts (see figure 28-16.)

Fault detected: (This happens when both end stations are set for manual configuration and both are set to MASTER or both are set to SLAVE.) Bit 10.15 of the 1000BASE-T Status Register is set to logical one to indicate that a manual configuration fault has been detected and bit 10:14 is set to logical one to indicate that MASTER-SLAVE resolution completed with a fault. Because the MASTER-SLAVE relationship was not established, link_status_1000BASE-T is set to FAIL, causing Auto-Negotiation to restart.

Note: MASTER-SLAVE arbitration only occurs if 1000BASE-T is selected as the HCD; otherwise it is assumed to have passed this condition.

40.6.2 Management Functions

The management interface specified in Clause 35 provides a simple, two wire serial interface to connect a management entity and a managed PHY for the purpose of controlling the PHY and gathering status from the PHY. This interface is referred to at the Gigabit Management Independent Interface (GMII.) The register definition specifies a basic register set with an extension mechanism.

1000BASE-T requires the basic register set that consists of two referred to as the Control Register (register 0) and the Status Register (register 1) and some PHY-specific registers. The detailed definitions of these registers are provided in 22.2.4.

The full set of management registers is listed in table 22-6; 1000BASE-T PHY-specific registers are listed in table 40-5

Table 40-4—100BASE-T2/1000BASE-T Control and Status registers

Register address	Register name	Basic/Extended
9	100BASE-T2/ 1000BASE-T Control register	E
‘0	100BASE-T2/ 1000BASE-T Status register	E

Table 40-5—100BASE-T2/1000BASE-T Control and Status registers

Register address	Register name	Basic/Extended
9	100BASE-T2/ 1000BASE-T Control register	E
‘0	100BASE-T2/ 1000BASE-T Status register	E

40.6.3 PHY specific registers for 1000BASE-T

Some of the extended registers (registers with addresses 2 to 15) are used as PHY specific registers as described in 22.2.4.2. A 1000BASE-T PHY shall use register addresses 9 and 10 for its control and status functions. The bits in the 1000BASE-T Control Register are used to place the PHY into several possible test modes and to determine the MASTER-SLAVE relationship during Auto-Negotiation as well as to provide for the advertisement of abilities. The bits in the 1000BASE-T Status Register are used to report the MASTER-SLAVE relationship determined during Auto-Negotiation, to report the local and remote receiver status, and to provide an idle error counter as well as the Link Partner’s advertised abilities.

40.6.3.1 1000BASE-T Control register (register 9)

Register 9 shall provide the following values for 1000BASE-T. The assignment of bits in the register is shown in table 40-6. The default value for each bit of the register should be chosen so that the initial state of the PHY upon power up or reset is normal operational state without management intervention.

Table 40-6—1000BASE-T Control Register (Address 9)

Bit	Name	Description	Type [1]
9.15	Test mode-bit 1	Default bit value is “0”	R/W
9.14	Test mode-bit 2	Default bit value is “0”	R/W
9.13	Test mode-bit 3	Default bit value is “0”	R/W
9.12	Master/Slave Config Enable	1=Enable MASTER-SLAVE Manual configuration value 0=Disable MASTER-SLAVE Manual configuration value	R/W
9.11	Master/Slave Config Value	1=Configure PHY as MASTER during MASTER-SLAVE negotiation, only when 9.12 is set to logical one. 0=Configure PHY as SLAVE during MASTER-SLAVE negotiation, only when 9.12 is set to logical one.	R/W
9.10	Repeater/ DTE	1=Repeater device port 0=DTE device	R/W
9.9	1000Base-T Full Duplex	1 = Advertise DTE is 1000BASE-T full duplex capable. 0 = Advertise DTE is not 1000BASE-T full duplex capable.	R/W
9.8	1000Base-T	1 = Advertise DTE is 1000BASE-T half duplex capable. 0 = Advertise DTE is not 1000BASE-T half duplex capable.	R/W
9.7	TX Coding	1 = Advertise to Link Partner to use 6dB transmit coding 0 = Advertise to Link Partner to use 3dB transmit coding	R/W
9.6	ASM_DIR	Advertise Asymmetric Pause direction bit. Se 37.4 for details. THis bit is used in conjunction with PAUSE.	R/W
9.5:0	Reserved	Reserved	R/W

1. R/W = Read/Write
RO = Read Only

40.6.3.1.1 Transmitter test mode

For a PHY with 1000BASE-T capability, the PHY shall be placed in transmitter test mode 1 operation (described in 40.7.1.1.2) when bit 9:15 is set to logical zero, bit 9:14 is set to logical zero and bit 9:13 is set to logical one. When bit 9:15 is set to logical zero, bit 9:14 is set to logical one and bit 9:13 is set to logical zero, the PHY shall be placed in transmitter test mode 2 operation as described in 40.7.1.1.2. When bit 9:15 is set to logical zero, bit 9:14 is set to logical one and bit 9:13 is set to logical zero, the PHY shall be placed in transmitter test mode 3 operation as described in 40.7.1.1.2. When bit 9:15 is set to logical one, bit 9:14 is set to logical zero and bit 9:13 is set to logical zero, the PHY shall be placed in transmitter test mode 4 operation as described in 40.7.1.1.2

The default value for bits 9.15:13 are all is zero.

40.6.3.1.2 MASTER-SLAVE Manual Configuration Enable

The MASTER-SLAVE relationship is established during Auto-Negotiation via either automatic MASTER-SLAVE configuration or manual configuration. If bit 9.12 is set to logical zero, then the MASTER-SLAVE configuration negotiation function will determine the PHY configuration. If bit 9.12 is set to logical one, then manual MASTER-SLAVE configuration shall be enabled, using bit 9.11 to specify the value. Usage of this bit is further described in 40.6.3.1.3.

The default value of bit 9.12 is zero.

40.6.3.1.3 MASTER-SLAVE Manual Configuration Value

MASTER-SLAVE Manual configuration is enabled by setting bit 9.12 to logical one. When manual configuration mode is enabled, setting bit 9.11 to logical zero configures the PHY as SLAVE during the MASTER-SLAVE negotiation process and shall be used to report the result of the MASTER-SLAVE configuration resolution for than PHY. Usage of this bit in MASTER_SLAVE configuration resolution is provided in 40.6.3.1.2.

The default value of bit 9.11 is zero.

40.6.3.1.4 Repeater/DTE Bit

Bit 9:10 shall be set to logical zero if the PHY is a DTE device and shall be set to logical one if the PHY is a repeater device port. Usage of this bit is described in 40.6.3.5.

40.6.3.1.5 1000BASE-T Full Duplex Advertise

Bit 9:9 shall be used to indicate the full duplex ability that will be advertised to the link partner. It will be used to determine the final operating speed in the priority resolution of Auto-Negotiation

40.6.3.1.6 .1000BASE-T Half Duplex Advertise

Bit 9:8 shall be used to indicate the half duplex ability that will be advertised to the link partner. It will be used to determine the final operating speed in the priority resolution of Auto-Negotiation.

40.6.3.1.7 TX_CODING

Bit 9:7 shall be used to determine what the link partner should use for its transmit coding method. Either 3dB or 6dB transmit coding can be selected. This bit is only relevant for 1000BASE-T.

40.6.3.1.8 ASM_DIR

Bit 9:6 shall be used to indicate the value for the asymmetric pause direction bit. For further information see 37.4.

40.6.3.1.9 Reserved bits

Bits 9:5.0 are reserved for future standardization. They shall be written as zero and shall be ignored when read. However, a PHY shall return the value zero in these bits.

40.6.3.2 100BASE-T2/1000BASE-T Status Register (register 10)

Register 10 shall provide the following values for 1000BASE-T. The assignment of bits in the register is shown in table 40-7. The default value for each bit of the register should be chosen so that the initial state of the PHY upon power up or reset is a normal operational state without management intervention.

Table 40-7—100BASE-T2/1000BASE-T Status Register (register 10) bit definition

Bit	Name	Description	Type [1]
10.15	MASTER-SLAVE manual configuration fault	1 = MASTER-SLAVE manual configuration fault detected 0 = No MASTER-SLAVE manual configuration fault detected	RO
10.14	MASTER-SLAVE configuration resolution complete	1 = MASTER-SLAVE configuration resolution has completed. 0 = MASTER-SLAVE configuration resolution has not completed	RO
10.13	Local Receiver Status	1 = Local Receiver OK 0 = Local Receiver not OK	RO
10.12	Remote Receiver Status	1 = Remote Receiver OK 0 = Remote Receiver not OK	RO
10:11	LP 1000T FD	1 = Link Partner is capable of 1000BASE-T full duplex 0 = Link Partner is not capable of 1000BASE-T full duplex	RO
10:10	LP 1000T HD	1 = Link Partner is capable of 1000BASE-T half duplex 0 = Link Partner is not capable of 1000BASE-T half duplex	RO
10:9	LP TX CODING	1 = Link Partner requests that 6dB coding be used 0 = Link Partner requests that 3dB coding be used	RO
10.8	ASM_DIR	Link Partner's Asymmetric Pause direction bit. Se 37.4 for details. THis bit is used in conjunction with PAUSE.	RO
10.7:0	Idle Error Count	Idle Error Count	RO/SC

1. R/W = Read/Write, RO = Read Only, SC = Self Clearing

40.6.3.2.1 MASTER-SLAVE Manual Configuration Fault

When read as a logical one, bit 10.15 indicates that a MASTER-SLAVE Manual Configuration Fault condition has been detected. The type of fault as well as the criteria and method of fault detection is PHY specific. The MASTER-SLAVE Manual Configuration Fault bit shall be implemented with a latching function, such that the occurrence of a MASTER-SLAVE Manual Configuration Fault will cause the MASTER-SLAVE Manual Configuration Fault bit to be set and remain set until it is cleared. The MASTER-SLAVE Manual Configuration Fault bit shall be cleared each time register 10 is read via the management interface and shall be cleared by a 1000BASE-T PMA reset. This bit will self clear on restart of auto negotiation or link failure. For l000BASE-T, this fault condition will occur when both PHYs are forced to be MASTER or SLAVE at the same time using bits 9.12 and 9.11. Bit 10.15 should be set via the MASTER-SLAVE Configuration Resolution function described in 40.6.3.5.

40.6.3.2.2 MASTER-SLAVE Configuration Resolution Complete

When read as a logical one, bit 10.14 indicates that the MASTER-SLAVE Resolution process has been completed and that the contents of registers 9 and 10 related to MASTER-SLAVE are valid. When read as a logic zero, bit 10.14 indicates that the MASTER-SLAVE Configuration Resolution process has not been completed and that the contents of registers 9 and 10 which are related to MASTER-SLAVE resolution are invalid. Bit 10.14 should be set via the MASTER-SLAVE Configuration Resolution function described in 40.6.3.5.

40.6.3.2.3 Local Receiver Status

Bit 10.13 indicates the status of the local receiver. Local receiver status is defined by the value of the bc_rcvr_status variable described in 40.4.4.1.

40.6.3.2.4 Remote Receiver Status

Bit 10.12 indicates the status of the remote receiver. Remote receiver status is defined by the value of the rem_rcvr_status variable described in 40.3.3.

40.6.3.2.5 LP 1000BASE-T FD

Bit 10.11 indicates the status of the Link Partners ability to perform 1000BASE-T Full Duplex operation. It is utilized by the priority resolution process to establish the link.

40.6.3.2.6 LP 1000BASE-T HD

Bit 10.10 indicates the status of the Link Partners ability to perform 1000BASE-T Half Duplex operation. It is utilized by the priority resolution process to establish the link.

40.6.3.2.7 LP TX CODING

Bit 10.9 indicates the status of the Link Partners desired TX coding method.

40.6.3.2.8 LP ASM_DIR

Bit 10.8 indicates the status of the Link Partners Asymmetric Pause Direction. See table 37.4

40.6.3.2.9 Idle Error Count

Bits 10.7:0 indicate the Idle Error count, where 10.7 is the most significant bit. During normal operation these bits contain a cumulative count of the errors detected when the receiver is receiving idles and the PHY Control parameter tx_mode is equal to SEND_N (indicating that both local and remote receiver status have been detected to be OK). When the PHY has receiver test mode (bit 9.13) enabled, these bits contain a cumulative count of the errors detected at all times when the local receiver status is OK. These bits are reset to all zeroes when the error count is read by the management function or upon execution of the PCS Reset function and they are held at all ones in case of overflow (see 30.5.1.1.11).

NOTE: REGISTER 15 is also utilized. It is the extended status register. It is currently defined in 802.3z.

40.6.3.3 Auto-Negotiation Pages Encoding

Auto-Negotiation enables a PHY to transmit and receive one or more pages of 16-bit Link Code Words with the remote PHY to exchange information for configuring the link. The first page transmitted in 802.3 systems is called the “base” page and is formatted as shown in Figure 40-20. Eight bits of the Base page are referred to as the Technology Ability Field (A[7:0]), containing information indicating which PHY technologies are supported by the PHY device. The current 802.3 Base page Technology Ability Field has 5 of its 8 bits defined in Table 28B-1 of the 100BASE-T standard, covering the 100BASE-TX, 100BASE-T4, and 10BASE-T PHYs. Because 1000BASE-T required more Auto-Negotiation bits than were available on the base page, bits for 1000BASE-T were defined using Next pages. Next pages come in two flavors, either Message or Unformatted Pages, shown in Figure 40-20. It is a requirement that all 1000BASE-T PHY implementations support the ability to process Next pages.

During 1000BASE-T PHY Auto-Negotiation, the Base page is followed with by a Message Next Page indicating that the pages that follow are specific to 1000BASE-T; this is signalled by using the Ability Message Code (7) defined in annex 28C. The Message Next Page is followed by two Unformatted Next Pages containing the 1000BASE-T Technology Specific parameters shown in table 40-8. Thus 1000BASE-T Auto-Negotiation typically requires transmission of four pages.

40.6.3.4 Use of Auto-Negotiation Next Page codes for 1000BASE-T PHYS

For a PHY capable of 1000BASE-T transmission, during Auto-Negotiation the Base Page will be followed by a Next Page with a message code containing the 1000BASE-T Technology Ability Message Code (9) as shown in table 28C-1. This Message Next Page indicates that two Unformatted Message Next Pages will follow which contain the 1000BASE-T Technology Ability fields as described in table 40-8. Further note that the Acknowledge 2 bit is not utilized and has no meaning when used for the 1000BASE-T message page exchange. All 1000BASE-TT Next Pages will be intercepted internal to the PHY and will not show up in the next page receive registers

Table 40-8—1000BASE-T Unformatted Next Pages bit assignments

Bit	Bit Definition	Register Location
PAGE 0		
10	Message Code (9)	Message Code (9)
9	Message Code (9)	
8	Message Code (9)	
7	Message Code (9)	
6	Message Code (9)	
5	Message Code (9)	
4	Message Code (9)	
3	Message Code (9)	
2	Message Code (9)	
1	Message Code (9)	
0	Message Code (9)	

PAGE 1		
10	Rsvd	Reserved
9	Rsvd	
8	Rsvd	
7	Rsvd	
6	Asymmetric_Pause value	GMII register 9.6 (1000BASE-T Control register)
5	TX_CODING (1 = 6dB and 0 = 3dB)	GMII register 9.7 (1000BASE-T Control register)
4	1000BASE-T half duplex (1 = half duplex and 0 = no half duplex)	GMII register 9.8 (1000BASE-T Control register)
3	1000BASE-T full duplex (1 = full duplex and 0 = no full duplex	GMII register 9.9 (1000BASE-T Control register)
2	1000BASE-T Repeater/DTE bit (1 = repeater and 0 = DTE)	GMII register 9.10 (1000BASE-T Control register)
1	1000BASE-T NASTER-SLAVE Manual Configuration value (1 = MASTER and 0 = SLAVE. This bit is ignored if U3 = 0.)	GMII register 9.11 (1000BASE-T Control register)
0	1000BASE-T MASTER-SLAVE Manual Configuration Enable (1 = Manual Configuration Enable.) This bit is intended to be used for manual selection in a a particular MASTER-SLAVE mode and is to be used in conjunction with bit U4.	GMII register 9.12 (1000BASE-T Control register)
Page 2		
10	1000BASE-T MASTER-SLAVE Seed Bit 10 (SB10) (MSB)	MASTER-SLAVE Seed Value (10:0)
9	1000BASE-T MASTER-SLAVE Seed Bit 9 (SB9)	
8	1000BASE-T MASTER-SLAVE Seed Bit 8 (SB8)	
7	1000BASE-T MASTER-SLAVE Seed Bit 7 (SB7)	
6	1000BASE-T MASTER-SLAVE Seed Bit 6 (SB6)	
5	1000BASE-T MASTER-SLAVE Seed Bit 5 (SB5)	
4	1000BASE-T MASTER-SLAVE Seed Bit 4 (SB4)	
3	1000BASE-T MASTER-SLAVE Seed Bit 3 (SB3)	

2	1000BASE-T MASTER-SLAVE Seed Bit 2 (SB2)	
1	1000BASE-T MASTER-SLAVE Seed Bit 1 (SB1)	
0	1000BASE-T MASTER-SLAVE Seed Bit 0 (SB0)	

40.6.3.5 MASTER-SLAVE Configuration Resolution

Since both PHYs that share a link segment are capable of being MASTER or SLAVE, a prioritization scheme exists to ensure that the correct mode is chosen. The MASTER-SLAVE relationship shall be determined during Auto-Negotiation using table 40-9 with the 1000BASE-T Technology Ability Next Page bit values specified in table 40-8 and information received from the link partner.

A 1000BASE-T PHY must be capable of operating either as the master or slave. In the scenario of a link between a DTE and a repeater, the preferred relationship is for the repeater to be the master PHY and the DTE to be the slave. However, other topologies may result in contention, and a resolution function is defined to resolve any relationship conflicts. This function is shown in table 40-9.

Table 40-9—1000BASE-T MASTER-SLAVE Configuration Resolution table

Local Device Type	Remote Link Partner Type	Resolution Function result	
		Local Device	Remote Link Partner
DTE (U2=0 & U3=0) or manual SLAVE (U3=1 & U4=0)	Repeater (U2 = 1 & U3=0) or manual MASTER (U3=1 & U4=1)	SLAVE	MASTER
Repeater (U2 = 1 & U3 = 0)	Manual MASTER (U3 = 1 & U4 = 1)		
Manual SLAVE (U3 = 1 & U4 = 0)	DTE (U2 = 0 & U3 = 0)		
Repeater (U2 = 1 & U3 = 0) or Manual MASTER (U3 = 1 and U4 = 1)	DTE (U2=0 & U3=0) or manual SLAVE (U3=1 & U4=0)	MASTER	SLAVE
DTE (U2 = 0 & U3 = 0)	Manual SLAVE (U3 = 1 & U4 = 0)		
Manual MASTER (U3 = 1 & U4 = 1)	Repeater (U2 = 1 & U3 = 0)		
Repeater (U2=1 & U3=0)	Repeater (U2=1 & U3=0)	PHY with higher MASTER-SLAVE seed value is configured as the MASTER. If the seeds are equal, the MASTER-SLAVE resolution is unsuccessful. Set link_status_T2 = FAIL, forcing Auto-Negotiation to restart.	
DTE (U2=0 & U3=0)	DTE (U2=0 & U3=0)		

Local Device Type	Remote Link Partner Type	Resolution Function result	
		Local Device	Remote Link Partner
Manual SLAVE (U3=1 & U4=0)	Manual SLAVE (U3=1 & U4=0)	Fault detected. Set link_status_T2 = FAIL, forcing Auto-Negotiation to restart.	
Manual MASTER (U3=1 & U4=1)	Manual MASTER (U3=1 & U4=1)		

The rationale for this hierarchy is straightforward. A 1000BASE-T repeater has higher priority than a DTE to become the MASTER. In the case where both devices are of the same type, e.g., both devices are Repeaters, the device with the higher MASTER-SLAVE seed bits (SB0..SB 10), where SB 15 is the MSB, becomes the MASTER and the device with the lower seed value becomes the SLAVE. In case both devices have the same seed value, both should assert link_status_1000T--FAIL (as defined in 28.3.1) and restart Auto-Negotiation. Successful completion of the MASTER-SLAVE resolution shall be treated as MASTER-SLAVE con-figuration resolution complete and the 1000BASE-T Status Register bit 10.14 shall be set to logical one.

The method of generating a random seed is left to the implementor. The generated random seeds should belong to a sequence of independent, identically distributed integer numbers with a uniform distribution in the range of 0 to XXXXX. The algorithm used to generate the integer should be designed to minimize the correlation between the number generated by any two devices at any given time. A seed counter shall be provided to track the number of seed attempts. The seed counter shall be set to zero at start-up and shall be incremented each time a seed is generated. A MASTER-SLAVE resolution fault shall be declared if resolution is not reached after the generation of seven seeds.

The MASTER-SLAVE Manual Configuration Enable bit (control register bit 9.12) is used to manually set a device to become the MASTER or the SLAVE. In case both devices are manually set to become the MASTER or the SLAVE, this condition shall be flagged as a MASTER-SLAVE Manual Configuration fault condition, thus the MASTER-SLAVE Manual Configuration fault bit (status register bit 10.15) shall be set to logical one. The MASTER-SLAVE Manual Configuration fault condition shall be treated as MASTER-SLAVE configuration resolution complete and status register bit 10.14 shall be set to logical one. In this case, link~status_10000BASE-T will be set to FAIL, because the MASTER-SLAVE relationship was not resolved. This will force Auto-Negotiation to restart after the link_fail_inhibit_timer has expired. Determination of MASTER-SLAVE values occur on the entrance to the FLP LINK GOOD CHECK state (figure 28-16) when the highest common denominator (HCD) technology is 1000BASE-T. The resulting MASTER-SLAVE value is used by the 1000BASE-T PHY control (40.3).

40.6.3.6 Priority Resolution

Since two devices may have multiple abilities in common, a prioritizing scheme exists to ensure that the highest common denominator ability is chosen. The following list represents the relative priorities of the technologies supported by the IEEE 802.3 Selector Field Value, where priorities are listed from highest to lowest. This list, from Annex 28B.3, is updated in table 40-10 to reflect the addition of the 1000BASE-T PHY as a supported technology for IEEE 802.3. 1000BASE-T is prioritized higher than 100BASE-T PHYs because it provides a higher level of performance.

This clause defines the electrical characteristics of the PHY at the MDI

Table 40-10—Priority Table

Priority Level	Technology
a ** (highest)	**1000BASE-T Full Duplex**
b**	**1000BASE-T Half Duplex**
c	100BASE-T2 Full Duplex
d	100BASE-TX Full Duplex
e	100BASE-T
f	100BASE-T4
g	100BASE-TX
h	10BASE-T Full Duplex
i (lowest)	10BASE-T
**** represents changes requested**	

40.7 PMA electrical specifications

The ground reference point for all common-mode tests is the GMII ground circuit. Implementations without an GMII use the chassis ground. The values of all components in test circuits shall be accurate to within ±1% unless otherwise stated.

40.7.1 PMA-to-MDI interface characteristics

40.7.1.1 Isolation requirement

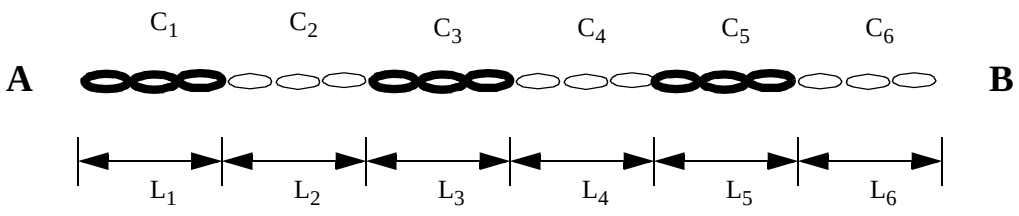
The PHY shall provide electrical isolation between the DTE or repeater circuits, including frame ground and all MDI leads. This electrical separation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC Publication 950.
b) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC Publication 950.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC Publication 60.

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC Publication 950, during the test. The resistance after the test shall be at least 2 Megaohms, measured at 500 Vdc.

40.7.1.1.1 Test channel

To perform the transmitter master/slave timing jitter tests described in this clause, a test channel is required to ensure that jitter is measured under conditions of poor signal to echo ratio. This test channel shall be constructed by combining 100 and 120 ohm cable segments which meet or exceed ISO/IEC 11801 category 5 specifications for each pair as shown in figure 40-16 with the lengths and additional restrictions on parameters described in table 40-11. The ends of the test channel shall be connectorized with connectors meeting or exceeding ISO/IEC 11801 category 5 specifications. The return loss of the resulting test channel shall meet the return loss requirements of 40.8.2.3 and the crosstalk requirements of 40.8.3 on each pair.



Identical for each of the 4 pairs.

Figure 40-16—Test Channel Topology For Each Cable Pair

Table 40-11—Test Channel Cable Segment Specifications

Cable Segment	Length (meters)	Characteristic Impedance (at frequencies > 1 MHz)	Attenuation (per 100 meters at 31.25 MHz)
1	L_1=1.20	120 +/- 5 ohms	7.8 to 8.8 dB
2	L_2=x	100 +/- 5 ohms	10.8 to 11.8 dB
3	L_3=1.48	120 +/- 5 ohms	7.8 to 8.8 dB
4	L_4=y	100 +/- 5 ohms	10.8 to 11.8 dB

Note: x is chosen such that the total delay of segments C1, C2 and C3 is equal to 570 ns at 31.25 MHz unless this would cause the total attenuation of segments C1, C2 and C3 to exceed the worst case insertion loss specified in 40.8.2.1 in which case x is chosen so that the total attenuation of segments C1, C2 and C3 just meets 40.8.2.1 at all frequencies. y is chosen so that the total attenuation of segments C1, C2, C3 and C4 just meets 40.8.2.1 at all frequencies (y may be 0).

40.7.1.1.2 Test modes

The test modes described below shall be provided to allow for testing of the transmitter waveform, transmitter distortion and transmitted jitter.

For a PHY with a GMII interface, these modes shall be enabled by setting bits 9:13-15 (1000BASE-T Control Register) of the GMII Management register set as shown in table 40-12 below. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal operation. A PHY without an GMII shall provide a means to provide these functions. The vendor shall provide a means to enable these modes for conformance testing.

Table 40-12— GMII management register settings for Test Modes

Bit 1 (9:15)	Bit 2 (9:14)	Bit 3 (9:13)	Mode
0	0	0	Normal Operation
0	0	1	Test Mode 1 - Transmit Waveform Test
0	1	0	Test Mode 2 - Transmit Jitter Test in MASTER mode
0	1	1	Test Mode 3 - Transmit Jitter Test in SLAVE mode
1	0	0	Test Mode 4 - Transmitter Distortion Test

When test mode 1 is enabled, the PHY shall transmit the following sequence of data symbols (TBD-Reference to PCS nomenclature for symbols) continually from all four transmitters:

{{+2 followed by 127 0 symbols}, {-2 followed by 127 0 symbols},{+1 followed by 127 0 symbols}, {-1 followed by 127 0 symbols}, {128 +2 symbols, 128 -2 symbols, 128 +2 symbols, 128 -2 symbols},{1024 0 symbols}}

This sequence is repeated continually without breaks between the repetitions when the test mode is enabled. A typical transmitter output is shown below in figure 40-17. The transmitter

time the transmitted symbols from a 125.000 MHz ± 0.01% clock in the MASTER timing mode.

When test mode 2 is enabled, the PHY shall transmit the data symbol sequence {+2,-2} repeatedly on all channels. The transmitter shall time the transmitted symbols from a 125.000 MHz ± 0.01% clock in the MASTER timing mode.

When test mode 3 is enabled, the PHY shall transmit the data symbol sequence {+2,-2} repeatedly on all channels. The transmitter shall time the transmitted symbols from a 125.000 MHz ± 1% clock in the SLAVE timing mode.

EDITOR'S NOTE: I don't like the above test mode much since the receive PLL is not locked to anything but I need a test that verifies that no jitter sources are introduced between TX-TCLK (see below) and the four transmitter outputs in the slave mode. Since the clocking is done differently in slave mode than master mode, I believe the slave test is required in addition to the master test. Alternate suggestions are encouraged.--JLC

When test mode 4 is enabled, the PHY shall transmit the sequence of symbols generated by the following scrambler generator polynomial, bit generation and level mappings:

$$g_{s1} = 1 + x^9 + x^{11}$$

The maximum-length shift register used to generate the sequences defined by this polynomial shall be updated once per symbol interval (8 ns). The bits stored in the shift register delay line at a particular time n are denoted by $Scr_n[11:0]$. The bit sequences, $x0_n$, $x1_n$ and $x2_n$, generated from combinations of the scrambler bits as shown below, shall be used to generate the quinary symbols, s_n, as shown in table 40-13. The quinary symbol sequence shall be presented simultaneously to all transmitters. The transmitter shall time the transmitted symbols from a 125,000 MHz ± 0.01% clock in the MASTER timing mode.

$$x1_n = Scr_n[1] \oplus Scr_n[4]$$

$$x0_n = Scr_n[0]$$

$$x2_n = Scr_n[2] \oplus Scr_n[4]$$

Table 40-13—Transmitter Test Mode 4 Symbol Mapping

x2n	x1n	x0n	quinary Symbol, s_n
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	-1
1	0	0	0
1	0	1	1
1	1	0	-2
1	1	1	-1

EDITOR'S NOTE: The above polynomials and mapping result in a level distribution where the +/-2 levels have 1/2 the probability of occurrence of any of the other levels. An alternate approach that results in equi-probable levels would be to use a single scrambler with a generator polynomial in GF(5) but it is not necessary for the purposes of this test.--JLC

Transmitter Test Mode Output

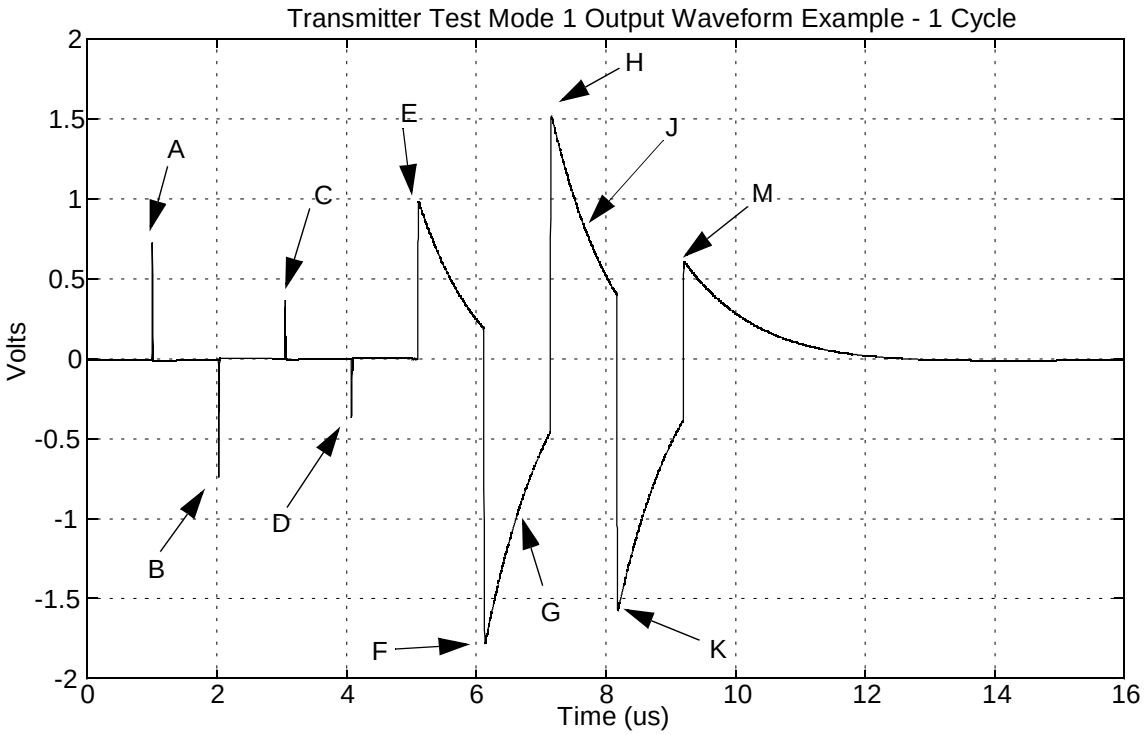


Figure 40-17—Example of Transmitter Test Mode 1 waveform

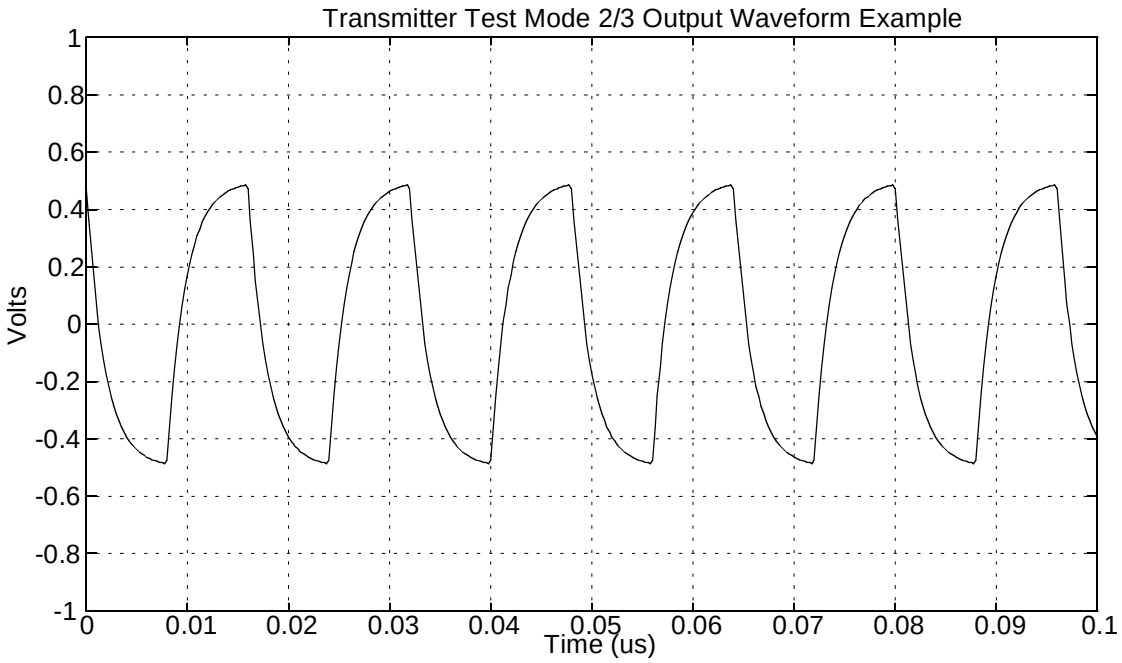


Figure 40-18—Example of Transmitter Test Modes 2 and 3 waveform

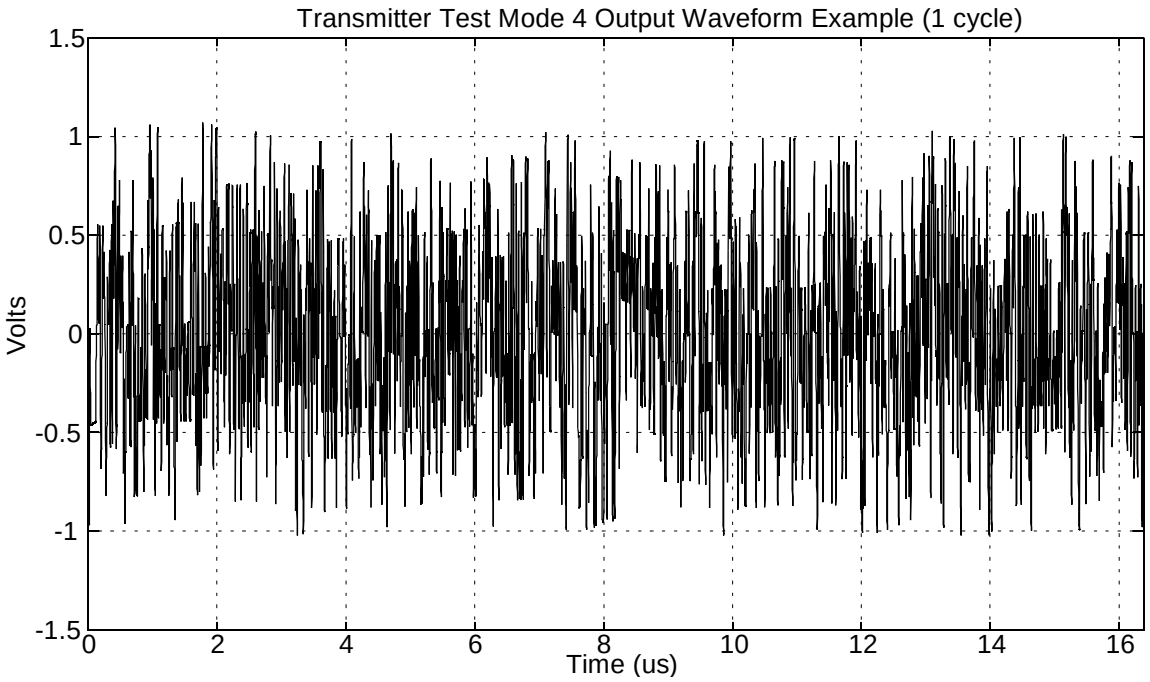


Figure 40-19—Example of Transmitter Test Mode 4 waveform

40.7.1.1.3 Test Fixtures

The following fixtures, or their functional equivalents, shall be used for measuring the transmitter specifications described later.

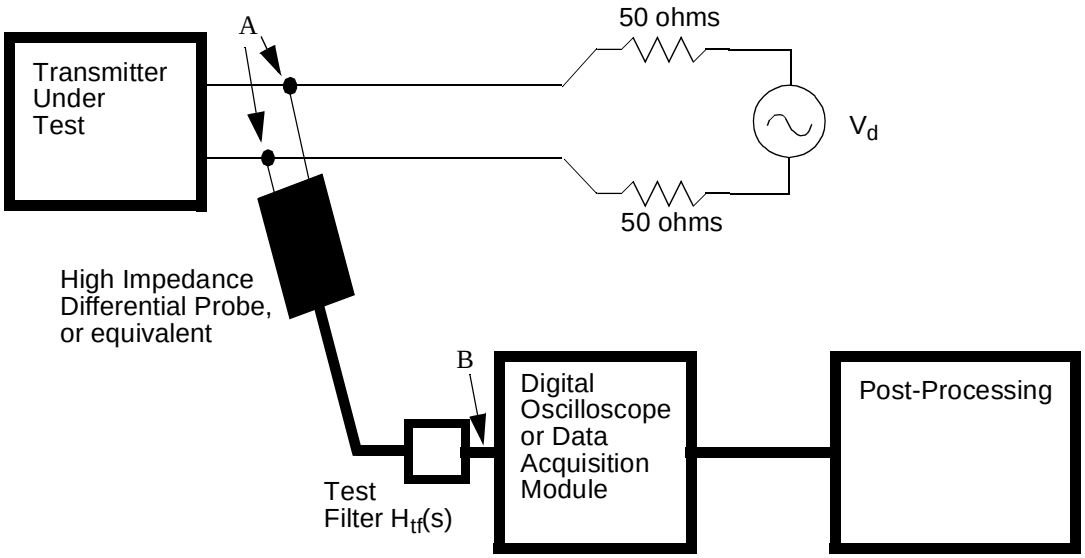


Figure 40-20—Transmitter Test Fixture 1 for Template Measurement

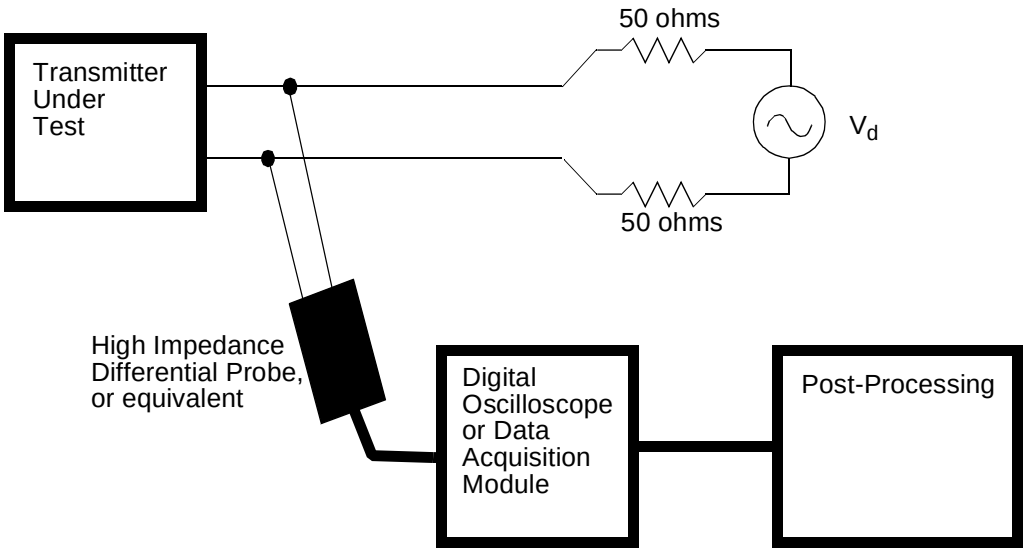


Figure 40-21—Transmitter Test Fixture 2 for Droop Measurement

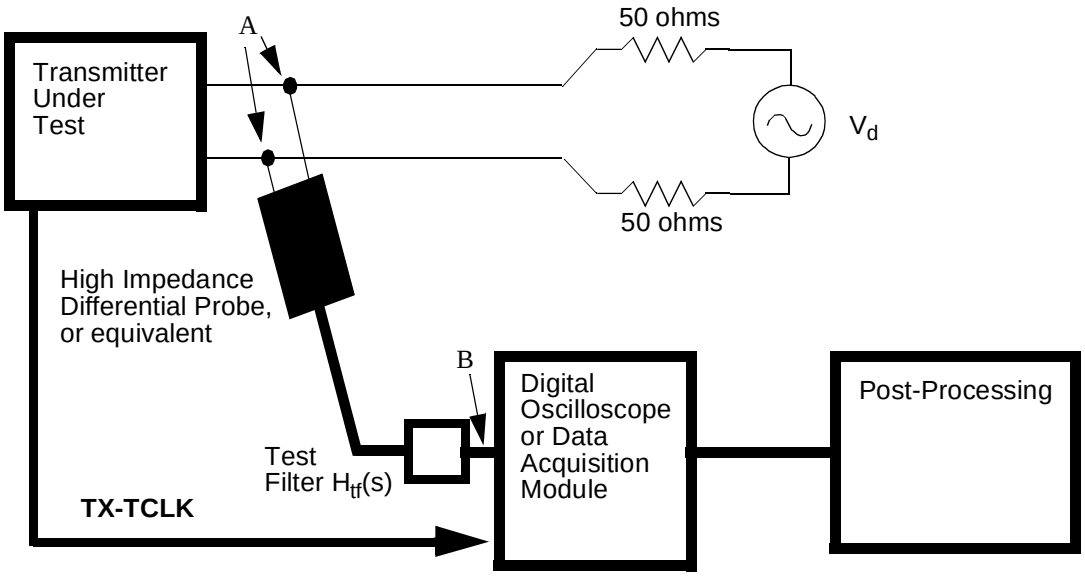


Figure 40-22—Transmitter Test Fixture 3 for Distortion Measurement

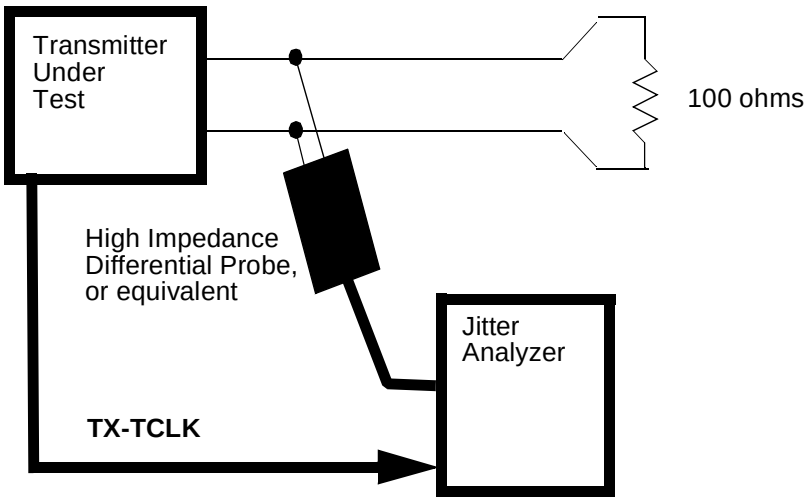


Figure 40-23—Transmitter Test Fixture 4 for Transmitter Jitter Measurement

The test filter, $H_{tf}(s)$, used in transmitter test fixtures 1 and 3 may be located between the points A and B as long as the test filter does not significantly alter the impedance seen by the transmitter. The test filter may instead be implemented as a digital filter in the post processing block. The test filter shall have the following continuous time transfer function or its discrete time equivalent[1]:

$$H_{tf}(f) = \frac{jf}{jf + 2\times10^{6}} \qquad f \text{ in Hz}$$

The disturbing signal, V_d, shall have the characteristics listed in table 40-14.

Table 40-14—Vd Characteristics

Characteristic	Transmit Test Fixture 1	Transmit Test Fixture 2	Transmit Test Fixture 3
Waveform	Sine wave		
Amplitude	7.0 volts peak-to-peak	7.0 volts peak-to-peak	8.0 volts peak-to-peak
Frequency	31.25 MHz	31.25 MHz	20.833 MHz (125/6 MHz)
Purity	All harmonics >40 dB below fundamental		

The post-processing block has two roles. The first is to remove the disturbing signal from the measurement. A method of removing the disturbing signal is to take a single shot acquisition of the transmitted signal plus test pattern then remove the best fit of a sine wave at the fundamental frequency of the disturbing signal from the measurement. It will be necessary to allow the fitting algorithm adjust the frequency (slightly), phase and amplitude parameters of the sine wave to achieve the best fit.

The second role of the post-processing block is to compare the measured data with the templates, droop specification or distortion specification.

Trigger averaging of the transmitter output to remove measurement noise and increase measurement resolution is acceptable provided that it is done in a manner that does not average out possible distortions caused by the interaction of the transmitter and the disturbing voltage. For transmitter template and droop measurements this can be done by ensuring that the disturbing signal is exactly synchronous to the test pattern so that the phase of the disturbing signal at any particular point in the test pattern remains constant[2]. Trigger averaging also requires a triggering event that is synchronous to the test pattern. A trigger pulse generated by the PHY would be ideal for this purpose; however, in practice, triggering off the waveform generated by one of the other transmitter outputs which does not have the disturbing signal present may be possible.

The generator of the disturbing signal must have enough linearity and range so that it does not introduce any appreciable distortion when connected to the transmitter output. This may be verified by replacing the trans-

1. j denotes the positive square root of -1
2. This may be accomplished by creating the disturbing signal using a source of the transmit clock for the PHY under test, dividing it down to the proper frequency for the disturbing signal, passing the result through a high Q bandpass filter to eliminate harmonics and then amplifying the result to the proper amplitude.

mitter under test with another, identical, disturbing signal generator with a different frequency output and verifying that the resulting waveform's spectrum does not show significant distortion products.

Additionally, to allow for measurement of transmitted jitter in master and slave modes, the PHY shall provide access to the 125 MHz symbol clock, TX-TCLK, that times the transmitted symbols. The PHY shall provide a means to enable this clock output if it is not normally enabled.

40.7.1.2 Transmitter electrical specifications

The PMA shall provide the Transmit function specified in 40.4.1.2 in accordance with the electrical specifications of this clause.

Where a load is not specified, the transmitter shall meet requirements of this clause with a 100 ohm resistive differential load connected to each transmitter output.

The tolerance on the poles of the test filters used in this section shall be ±1%.

Practical considerations prevent measurement of the transmitter performance in the presence of the remote transmitter signal in this standard; however, the design of the transmitter to tolerate the presence of the remote transmitter signal without unacceptable distortion or other changes in performance is a critical issue and must be addressed by the manufacturer. To this end, a disturbing sine wave is used to simulate the presence of a remote transmitter for a number of the transmitter tests below.

40.7.1.2.1 Peak differential output voltage and level accuracy

When in test mode 1 and observing the differential signal output at the MDI using transmitter test fixture 1, for each pair, with no intervening cable, the absolute value of the peak of the waveform at points A and B as defined in figure 40-17 shall fall within the range of 0.67 V to 0.82 V (0.75 V ± 0.83 dB).

EDITOR'S NOTE: This specification is consistent with the desire for a 2 volt peak-to-peak launch level (in the absence of baseline wander) since the +2 symbol corresponding normally to a +1 volt level is filtered by the partial response filter $0.75+0.25z^{-1}$ which means that an isolated +2 symbol will generate +0.75 volts for one symbol time followed by +0.25 volts for a subsequent symbol time.--JLC

The absolute value of the peak of the waveforms at points A and B shall differ by less than 1%.

The absolute value of the peak of the waveform at points C and D as defined in figure 40-17 shall differ from 0.5 times the average of the absolute values of the peaks of the waveform at points A and B by less than 2%.

40.7.1.2.2 Maximum output droop

When in test mode 1 and observing the differential signal output at the MDI using transmit test fixture 2, for either pair, with no intervening cable, the magnitude of the negative peak value of the waveform at point G as defined in figure 40-17 shall be greater than 73.1% of the magnitude of the negative peak value of the waveform at point F. Point G is defined as the point exactly 500 ns after point F. Point F is defined as the point where the waveform reaches it's minimum value at the location indicated in figure 40-17. Additionally, the magnitude of the peak value of the waveform at point J as defined in figure 40-17 shall be greater than 73.1% of the magnitude of the peak value of the waveform at point H. Point J is defined as the point exactly 500 ns after point H. Point H is defined as the point where the waveform reaches it's maximum value at the location indicated in figure 40-17.

EDITOR'S NOTE: This specification is designed to limit the high pass filtering of the transmitter/transformer to the equivalent of a single pole high pass filter with a pole frequency less than or equal to 100 kHz.--JLC

40.7.1.2.3 Differential output templates

When in test mode 1 and observing the differential signal output at the MDI using transmitter test fixture 1, for each pair, with no intervening cable, the voltage waveforms at points A, B, C, D defined in figure 40-17, after the normalization described below, shall lie within the time domain template 1 defined in figure 40-24 and the piecewise linear interpolation between the points in table 40-15. The waveforms may be shifted in time as appropriate to fit within the template.

The waveform at point A is normalized by dividing by the peak value of the waveform at A.

The waveform at point B is normalized by dividing by the negative of the peak value of the waveform at A.

The waveform at point C is normalized by dividing by 1/2 the peak value of the waveform at A.

The waveform at point D is normalized by dividing by the negative of 1/2 the peak value of the waveform at A.

When in test mode 1 and observing the differential signal output at the MDI using transmitter test fixture 1, for each pair, with no intervening cable, the voltage waveforms at points F and H defined in figure 40-17, after the normalization described below, shall lie within the time domain template 2 defined in figure 40-24 and the piecewise linear interpolation between the points in table 40-16. The waveforms may be shifted in time as appropriate to fit within the template.

The waveform at point F is normalized by dividing by the peak value of the waveform at F.

The waveform at point H is normalized by dividing by the peak value of the waveform at H.

<EDITOR'S NOTE: The templates were created with the following assumptions about the elements in the transmit path:

Digital Filter: $0.75 + 0.25\ z^{-1}$

Ideal DAC

Single pole continuous time low pass filter with pole varying from 70.2 MHz to 117 MHz.

Single pole continuous time high pass filter (transformer high pass) with pole varying from 1 Hz to 100 kHz.

Single pole continuous time high pass filter (test filter) with pole varying from 1.8 MHz to 2.2 MHz (I could tighten this to a 1% variation...).

Additionally, +0.02 was added to the upper template and -0.02 was added to the lower template to allow for noise and measurement error.

--JLC>

NOTE—The transmit templates are not intended to address electromagnetic radiation limits.

Normalized Time Domain Transmit Template

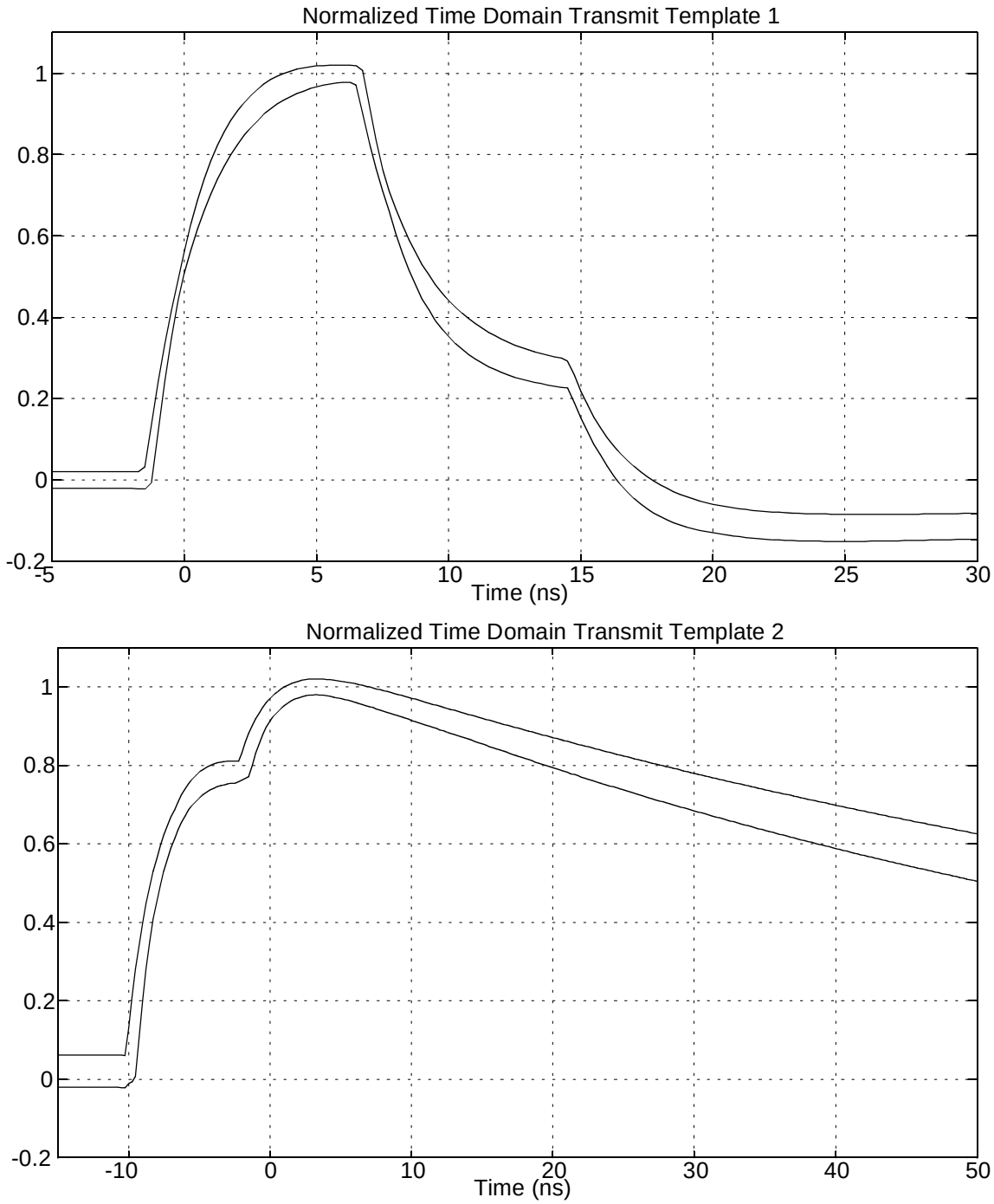


Figure 40-24—Normalized transmit templates as measured at MDI using Transmit Test Fixture 1

Table 40-15— Normalized Time Domain Voltage Template 1

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
-5.00	0.025	-0.026	12.75	0.332	0.210
-4.75	0.025	-0.026	13.00	0.326	0.208
-4.50	0.025	-0.026	13.25	0.320	0.206
-4.25	0.025	-0.026	13.50	0.315	0.204
-4.00	0.025	-0.026	13.75	0.311	0.202
-3.75	0.025	-0.026	14.00	0.307	0.201
-3.50	0.025	-0.026	14.25	0.303	0.199
-3.25	0.025	-0.026	14.50	0.300	0.186
-3.00	0.025	-0.026	14.75	0.292	0.148
-2.75	0.025	-0.026	15.00	0.278	0.114
-2.50	0.025	-0.026	15.25	0.254	0.084
-2.25	0.026	-0.026	15.50	0.200	0.041
-2.00	0.026	-0.027	15.75	0.157	0.006
-1.75	0.037	-0.027	16.00	0.128	-0.023
-1.50	0.141	-0.028	16.25	0.104	-0.048
-1.25	0.247	-0.028	16.50	0.083	-0.068
-1.00	0.339	-0.028	16.75	0.064	-0.084
-0.75	0.422	-0.006	17.00	0.047	-0.098
-0.50	0.496	0.152	17.25	0.032	-0.110
-0.25	0.584	0.304	17.50	0.019	-0.119
0.00	0.669	0.427	17.75	0.007	-0.127
0.25	0.739	0.505	18.00	-0.004	-0.133
0.50	0.796	0.563	18.25	-0.014	-0.138
0.75	0.844	0.614	18.50	-0.022	-0.143
1.00	0.882	0.660	18.75	-0.030	-0.146
1.25	0.914	0.701	19.00	-0.037	-0.149
1.50	0.940	0.737	19.25	-0.043	-0.151
1.75	0.960	0.769	19.50	-0.048	-0.153

Table 40-15— Normalized Time Domain Voltage Template 1

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
2.00	0.977	0.797	19.75	-0.053	-0.154
2.25	0.990	0.822	20.00	-0.057	-0.155
2.50	1.001	0.845	20.25	-0.061	-0.156
2.75	1.008	0.864	20.50	-0.064	-0.157
3.00	1.015	0.881	20.75	-0.067	-0.157
3.25	1.019	0.896	21.00	-0.070	-0.158
3.50	1.022	0.909	21.25	-0.072	-0.158
3.75	1.024	0.921	21.50	-0.074	-0.158
4.00	1.025	0.931	21.75	-0.076	-0.158
4.25	1.025	0.939	22.00	-0.077	-0.158
4.50	1.025	0.946	22.25	-0.078	-0.158
4.75	1.025	0.953	22.50	-0.079	-0.158
5.00	1.025	0.958	22.75	-0.079	-0.157
5.25	1.025	0.962	23.00	-0.079	-0.157
5.50	1.025	0.966	23.25	-0.080	-0.157
5.75	1.025	0.966	23.50	-0.080	-0.157
6.00	1.025	0.964	23.75	-0.080	-0.156
6.25	1.025	0.960	24.00	-0.080	-0.156
6.50	1.025	0.897	24.25	-0.080	-0.156
6.75	1.025	0.826	24.50	-0.080	-0.156
7.00	1.014	0.763	24.75	-0.080	-0.156
7.25	0.996	0.707	25.00	-0.080	-0.156
7.50	0.888	0.642	25.25	-0.080	-0.156
7.75	0.784	0.570	25.50	-0.080	-0.156
8.00	0.714	0.510	25.75	-0.079	-0.156
8.25	0.669	0.460	26.00	-0.079	-0.156
8.50	0.629	0.418	26.25	-0.079	-0.156
8.75	0.593	0.383	26.50	-0.079	-0.155
9.00	0.561	0.354	26.75	-0.079	-0.155

Table 40-15— Normalized Time Domain Voltage Template 1

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
9.25	0.533	0.330	27.00	-0.078	-0.155
9.50	0.507	0.309	27.25	-0.078	-0.155
9.75	0.483	0.292	27.50	-0.078	-0.154
10.00	0.462	0.278	27.75	-0.078	-0.154
10.25	0.443	0.266	28.00	-0.077	-0.154
10.50	0.427	0.255	28.25	-0.077	-0.153
10.75	0.411	0.247	28.50	-0.077	-0.153
11.00	0.398	0.239	28.75	-0.076	-0.153
11.25	0.385	0.233	29.00	-0.076	-0.152
11.50	0.374	0.228	29.25	-0.076	-0.152
11.75	0.364	0.223	29.50	-0.076	-0.152
12.00	0.355	0.219	29.75	-0.075	-0.151
12.25	0.346	0.216	30.00	-0.075	-0.151
12.50	0.339	0.213			

Table 40-16— Normalized Time Domain Voltage Template 2

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
-15.00	0.066	-0.025	18.00	0.891	0.790
-14.50	0.066	-0.025	18.50	0.886	0.784
-14.00	0.066	-0.025	19.00	0.881	0.778
-13.50	0.066	-0.025	19.50	0.876	0.772
-13.00	0.066	-0.025	20.00	0.871	0.767
-12.50	0.066	-0.025	20.50	0.866	0.761
-12.00	0.066	-0.025	21.00	0.861	0.755
-11.50	0.066	-0.025	21.50	0.856	0.750
-11.00	0.066	-0.025	22.00	0.852	0.744
-10.50	0.066	-0.025	22.50	0.847	0.738

Table 40-16— Normalized Time Domain Voltage Template 2

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
-10.00	0.216	-0.027	23.00	0.842	0.733
-9.50	0.348	-0.027	23.50	0.838	0.727
-9.00	0.452	-0.013	24.00	0.833	0.722
-8.50	0.535	0.130	24.50	0.828	0.717
-8.00	0.604	0.347	25.00	0.824	0.711
-7.50	0.683	0.490	25.50	0.819	0.706
-7.00	0.737	0.557	26.00	0.815	0.701
-6.50	0.772	0.610	26.50	0.811	0.695
-6.00	0.795	0.651	27.00	0.806	0.690
-5.50	0.810	0.683	27.50	0.802	0.685
-5.00	0.818	0.707	28.00	0.797	0.680
-4.50	0.823	0.725	28.50	0.793	0.675
-4.00	0.825	0.739	29.00	0.789	0.670
-3.50	0.826	0.747	29.50	0.784	0.665
-3.00	0.825	0.752	30.00	0.780	0.660
-2.50	0.823	0.755	30.50	0.776	0.655
-2.00	0.864	0.755	31.00	0.772	0.650
-1.50	0.907	0.758	31.50	0.767	0.645
-1.00	0.941	0.760	32.00	0.763	0.640
-0.50	0.966	0.803	32.50	0.759	0.635
0.00	0.986	0.870	33.00	0.755	0.630
0.50	1.001	0.914	33.50	0.751	0.626
1.00	1.014	0.941	34.00	0.747	0.621
1.50	1.022	0.954	34.50	0.743	0.616
2.00	1.025	0.964	35.00	0.739	0.611
2.50	1.025	0.970	35.50	0.734	0.607
3.00	1.025	0.973	36.00	0.730	0.602
3.50	1.025	0.969	36.50	0.727	0.598
4.00	1.025	0.965	37.00	0.723	0.593

Table 40-16— Normalized Time Domain Voltage Template 2

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
4.50	1.023	0.960	37.50	0.719	0.589
5.00	1.020	0.955	38.00	0.715	0.584
5.50	1.017	0.949	38.50	0.711	0.580
6.00	1.014	0.942	39.00	0.707	0.575
6.50	1.010	0.936	39.50	0.703	0.571
7.00	1.005	0.929	40.00	0.699	0.566
7.50	1.001	0.922	40.50	0.695	0.562
8.00	0.996	0.916	41.00	0.692	0.558
8.50	0.991	0.909	41.50	0.688	0.554
9.00	0.986	0.903	42.00	0.684	0.549
9.50	0.981	0.896	42.50	0.680	0.545
10.00	0.976	0.889	43.00	0.677	0.541
10.50	0.970	0.883	43.50	0.673	0.537
11.00	0.965	0.876	44.00	0.669	0.533
11.50	0.960	0.870	44.50	0.666	0.529
12.00	0.954	0.864	45.00	0.662	0.524
12.50	0.949	0.857	45.50	0.659	0.520
13.00	0.944	0.851	46.00	0.655	0.516
13.50	0.938	0.845	46.50	0.651	0.512
14.00	0.933	0.838	47.00	0.648	0.508
14.50	0.928	0.832	47.50	0.644	0.505
15.00	0.923	0.826	48.00	0.641	0.501
15.50	0.917	0.820	48.50	0.637	0.497
16.00	0.912	0.814	49.00	0.634	0.493
16.50	0.907	0.808	49.50	0.631	0.489
17.00	0.902	0.802	50.00	0.627	0.485
17.50	0.897	0.796			

40.7.1.2.4 Transmitter Distortion

Editor's Note: The status and location of the MATLAB code shown below is in resolution and the code may be moved, depending on the outcome of the resolution process.

When in test mode 4 and observing the differential signal output at the MDI using transmitter test fixture 3, for each pair, with no intervening cable, the peak distortion as defined below shall be less than 10 millivolts.

The peak distortion is determined by sampling the differential signal output with the symbol rate TX-TCLK at an arbitrary phase and processing a block of any 2047 consecutive samples with the Matlab code listed below or equivalent. Note that this code assumes that the differential signal has already been filtered by the test filter.

MATLAB code for Distortion Post Processing

```
%
% Distortion Specification Post Processing
%   V1.3 (uses single scrambler instead of 3)
%

% Initialize Variables
clear
symbolRate=125e6;                    % symbol rate
dataFile=input('Data file name: ','s')

% Generate test pattern symbol sequence

scramblerSequence=ones(1,2047);
for i=12:2047
 scramblerSequence(i)=mod(scramblerSequence(i-11) + scramblerSequence(i-9),2);
end

for i=1:2047
 temp=scramblerSequence(mod(i-1,2047)+1) + ...
    2*mod(scramblerSequence(mod(i-2,2047)+1) + scramblerSequence(mod(i-5,2047)+1),2) + ...
    4*mod(scramblerSequence(mod(i-3,2047)+1) + scramblerSequence(mod(i-5,2047)+1),2);
 switch temp
   case 0,
     testPattern(i)=0;
   case 1,
     testPattern(i)=1;
   case 2,
     testPattern(i)=2;
   case 3,
     testPattern(i)=-1;
   case 4,
     testPattern(i)=0;
   case 5,
     testPattern(i)=1;
   case 6,
     testPattern(i)=-2;
   case 7,
     testPattern(i)=-1;
 end
end
```

```
% Input data file
fid=fopen(dataFile,'r');
sampledData=fscanf(fid,'%f');
fclose(fid);
sampledData=sampledData.';

if (length(sampledData) < 2047)
  error('Must have 2047 consecutive samples for processing');
elseif (length(sampledData) > 2047)
  fprintf(1,'\n Warning - only using first 2047 samples in data file');
  sampledData=sampledData(1:2047);
end


% Fit a sine wave to the data and temporarily remove it to yield processed data

options=foptions;
options(1)=0;
options(2)=1e-8;
options(3)=1e-8;
options(14)=2000;
gradfun=zeros(0);
P=fmins('sinefit',[2.0 0 125/6.],options,gradfun,sampledData,symbolRate);

P

processedData=sampledData - ...
    P(1)*sin(2*pi*(P(3)*1e6*[0:2046]/symbolRate + P(2)*1e-9*symbolRate));



% LMS Canceller

numberCoeff=70;  % Number of coefficients in canceller
coefficients=zeros(1,numberCoeff);
delayLine=testPattern;

% Align data in delayLine to sampled data pattern
temp=xcorr(processedData,delayLine);
index=find(abs(temp)==max(abs(temp)));
index=mod(mod(length(processedData) - index(1),2047)+numberCoeff-10,2047);
delayLine=[delayLine((end-index):end) delayLine(1:(end-index-1))];


% Compute coefficients that minimize squared error in cyclic block

for i=1:2047
  X(i,:)=delayLine(mod([0:(numberCoeff-1)]+i-1,2047)+1);
end
coefficients=(inv(X.' * X)*(processedData*X).').';



% Canceller
for i=1:2047
  err(i)=processedData(i) - sum(delayLine(1+mod((i-1):(i+numberCoeff-2),2047)).*coefficients);
end

% Add back temporarily removed sine wave

err=err+P(1)*sin(2*pi*(P(3)*1e6*[0:2046]./symbolRate + P(2)*1e-9*symbolRate));
```

```
% Re-fit sine wave and do a final removal

options=foptions;
options(1)=0;
options(2)=1e-12;
options(3)=1e-12;
options(14)=10000;
gradfun=zeros(0);
P=fmins('sinefit',[2.0 0 125/6.],options,gradfun,err,symbolRate);

P

processedData=sampledData - ...
   P(1)*sin(2*pi*(P(3)*1e6*[0:2046]/symbolRate + P(2)*1e-9*symbolRate));


% Compute coefficients that minimize squared error in cyclic block

coefficients=(inv(X.' * X)*(processedData*X).').';



% Canceller
for i=1:2047
  err(i)=processedData(i) - sum(delayLine(1+mod((i-1):(i+numberCoeff-2),2047)).*coefficients);
end

% SNR Calculation
signal=0.5;
noise=mean(err.^2);

SNR=10*log10(signal./noise);

% Output Peak Distortion

peakDistortion=max(abs(err))


% Function for fitting sine wave
function err=sinefit(parameters,data,symbolRate)
err=sum((data- ...
        parameters(1)*sin(2*pi*(parameters(3)*1e6*[0:(length(data)-1)]/symbolRate + parameters(2)*1e-9*symbol-
Rate))).^2);
```

40.7.1.2.5 Transmitter Timing Jitter

When in test mode 2 or test mode 3, the peak-to-peak jitter of the zero crossings of the differential signal output at the MDI relative to the corresponding edge of TX-TCLK shall be less than 0.100 ns for each transmitter. The corresponding edge of TX-TCLK is the edge of the transmit test clock, in polarity and time, that generates the zero-crossing transition being measured.

When in the normal mode of operation as the master, receiving valid signal from a compliant PHY operating as the slave using the test channel defined in 40.7.1.1.1, with test channel port B connected to the slave, the peak-to-peak value of the slave TX-TCLK jitter relative to the master TX-TCLK shall be less than 2.4 ns after the receiver is properly receiving the data and has set bit TBD of the GMII management register set to

1. When the jitter waveform on TX_TCLK is filtered by a high pass filter, $H_{jf1}(f)$ having the transfer function below[1], the peak-to-peak value of the resulting filtered timing jitter shall be less than 0.250 ns.

$$H_{jf1}(f) = \frac{jf}{jf + 75000} \qquad f \text{ in Hz}$$

When in the normal mode of operation as the slave, receiving valid signal from a compliant PHY operating as the master using the test channel defined in 40.7.1.1.1, with test channel port A connected to the slave, the peak-to-peak value of the master TX-TCLK jitter relative to an unjittered reference shall be less than 2.4 ns after the receiver is properly receiving the data and has set bit TBD of the GMII management register set to 1. When the jitter waveform on TX_TCLK is filtered by a high pass filter, $H_{jf2}(f)$, having the transfer function below, the peak-to-peak value of the resulting filtered timing jitter shall be less than 0.250 ns greater than the simultaneously measured peak-to-peak value of the master jitter filtered by $H_{jf1}(f)$.

.

$$H_{jf2}(f) = \frac{jf}{jf + 1500} \qquad f \text{ in Hz}$$

For all jitter measurements the peak-to-peak value shall be measured over an unbiased sample of 10^{10} clock edges.

40.7.1.2.6 Transmit clock frequency

The quinary symbol transmission rate on each pair shall be 125.000 MHz ± 0.01%.

40.7.1.3 Receiver electrical specifications

The PMA shall provide the Receive function specified in 40.4.1.3 in accordance with the electrical specifications of this clause. The patch cabling and interconnecting hardware used in test configurations shall meet or exceed ISO/IEC 11801 category 5 specifications.

40.7.1.3.1 Receiver differential input signals

Differential signals received on the receive inputs that were transmitted within the specifications given in 40.7.1.2, and have then passed through any link compatible with Clause 40, shall be translated into one of the PMA_UNITDATA.indicate messages with an 4-D symbol error rate less than 10^{-10} and sent to the PCS after link bring-up. Since the 4-D symbols are not accessible, this specification shall be satisfied by packet error rate less than 10^{-7} for 1000 byte packets.

---

1. "j" denotes the positive square root of -1.

40.7.1.3.2 Receiver frequency tolerance

The receive feature shall properly receive incoming data with a 5-level symbol rate within the range 125.000 MHz ± 0.01%.

40.7.1.3.3 Common-mode noise rejection

While receiving packets from a compliant 1000BASE-T transmitter, connected to all MDI pins, a receiver shall send the proper PMA_UNITDATA.indicate messages to the PCS for any differential input signal E_s that results in a signal E_{dif} that meets 40.7.1.3.1 even in the presence of common mode voltages E_{cm} (applied as shown in Figure 40-25—). E_{cm} shall be a 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%-80%), connected to each of the pairs.

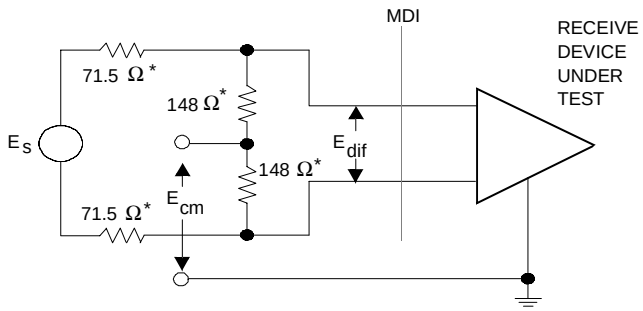


Figure 40-25—Receiver common-mode noise rejection test

40.7.1.4 MDI Specifications

40.7.1.4.1 MDI differential impedance

The differential impedance as measured at the MDI for each transmit/receive channel shall be such that any reflection due to differential signals incident upon the MDI from a balanced cabling having an impedance of 100 ohms is at least 17 dB below the incident signal over the frequency range of 2.0 MHz to 31.25 MHz and at least 12.9 - $20\log_{10}(f/50)$ dB over the frequency range 31.25 MHz to 125 MHz (f in MHz). This return loss shall be maintained at all times when the PHY is transmitting data.

<EDITOR'S Note - this is a scaled version of the T2 spec and is consistent with the return loss of the Pulse Inc. presentation "KEA 4.0 Second Generation 1000BaseT Hybrid Transformer" by Henry Hinrichs>--JLC

40.7.1.4.2 MDI impedance balance

Over the frequency range 2.0 MHz to 125.0 MHz the common-mode to differential-mode impedance balance of each channel of the MDI shall exceed:

where f is the frequency in MHz when the transmitter is transmitting random or pseudo random data. Test mode 4 may be used to generate an appropriate transmitter output.

The balance is defined as:

$$29 - 17\log\left(\frac{f}{50}\right) \quad \text{dB}$$

$$20\log\left(\frac{E_{cm}}{E_{dif}}\right)$$

where E_{cm} is an externally applied sine wave voltage as shown in figure 40-26 and E_{dif} is the resulting waveform due only to the applied sine wave and not the transmitted data[1].

NOTE—The balance of the test equipment (such as the matching of the test resistors) must be insignificant relative to

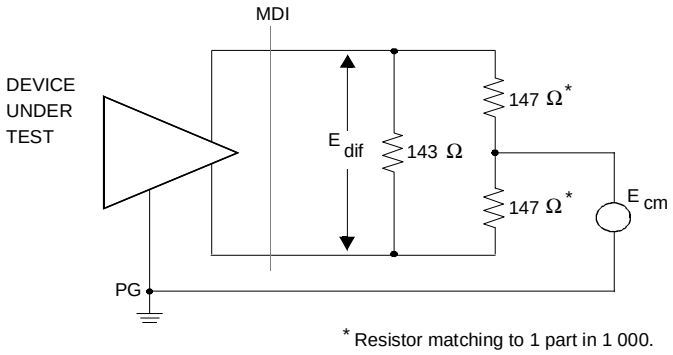


Figure 40-26—MDI impedance balance test circuit

the balance requirements.

<EDITOR'S Note - this is a scaled version of the T2 spec and is consistent with the return loss of the Pulse Inc. presentation "KEA 4.0 Second Generation 1000BaseT Hybrid Transformer" by Henry Hinrichs>--JLC

40.7.1.4.3 MDI common-mode output voltage

The implementor should consider any applicable local, national, or international regulations. Driving balanced cable pairs with high-frequency common mode voltages may cause radiated emissions which may result in interference to other equipment. FCC conducted and radiated emissions tests may require that the

1. Triggered averaging can be used to separate the component due to the applied common mode sine wave from the transmitted data component.

magnitude of the total common mode output voltage, E_{cm_out}, on any transmit circuit, when measured as shown in figure 40-27, be less than a few millivolts when transmitting data.

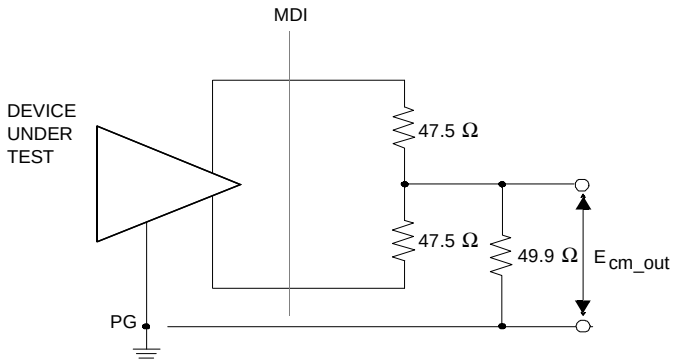


Figure 40-27—Common-mode output voltage test circuit

NOTE—The balance of the test equipment (such as the matching of the test resistors) must be insignificant relative to the balance requirements.

40.7.1.4.4 MDI fault tolerance

Transmitters and receivers shall withstand without damage the application of short circuits across any MDI port for an indefinite period of time and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

Transmitters shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in figure 40-28). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC Publication 60.

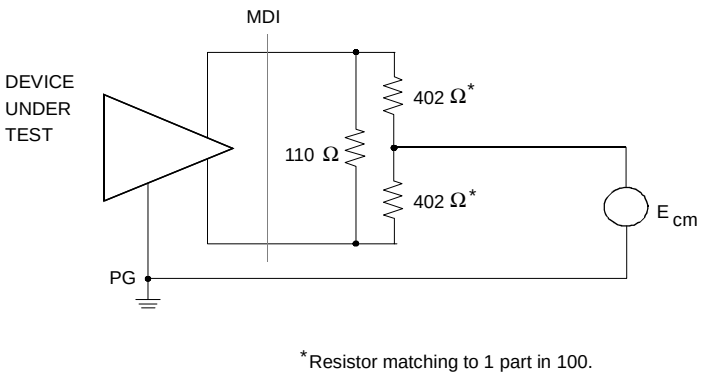


Figure 40-28—MDI fault tolerance test circuit

40.8 Link Segment Characteristics

1000BASE-T uses a duplex transmission system. Four full duplex channels are required to transport data between two PMDs. Each duplex channel supports an effective data rate of 250 Mbps in each direction simultaneously. The term 'link segment' used in this clause refers to four duplex channels and the term 'duplex channel' will be used to refer a single channel with full duplex capability. Specifications for a link segment applies equally to each for the four duplex channels.

1000BASE-T is designed to operate over a 4-pair Category 5 cabling system.

40.8.1 Cabling System Characteristics

The cabling system used to support 1000BASE-T requires 4 pairs of Category 5 balanced cabling with a nominal impedance of 100 ohms. The cabling system components (cables, cords and connectors) used to provide the link segment shall consist of Category 5 components as specified in ISO/IEC 11801:1995.

a) 1000BASE-T uses a star topology with category 5 balanced cabling used to connect PHY entities. b) 1000BASE-T is an ISO/IEC 11801 Class D application, with additional installation requirements and transmission parameters specified in _____. c) The width of the PMD transmit signal spectrum is ____ MHz. d) The use of shielding is outside the scope of this standard.

40.8.2 Link Transmission Parameters

The transmission parameters contained in this section are specified to ensure a Category 5 link segment of at least 100 meters will provide a reliable transmission media for 1000BASE-T. The transmission parameters include insertion loss, link delay, characteristic impedance, NEXT loss, ELFEXT loss and return loss.

Unless otherwise specified, link segment testing shall be conducted using source and load impedance's of 100 ohms. Also, the tolerance on the poles of the test filter used in this section shall be 1%.

40.8.2.1 Insertion Loss

The insertion loss of each duplex channel shall be less than

$$\text{Insertion\_Loss}(f) < 2.1\, f^{0.529} + 0.4/f \quad \text{(dB)}$$

at all frequencies from 1 to 100 MHz[1]. This includes the attenuation of the balanced cabling pairs, connector losses, and patch cord losses of the duplex channel. The insertion loss specification shall be met when the duplex channel is terminated in 100 ohms.

40.8.2.2 Differential Characteristic Impedance

The nominal differential impedance of each link segment duplex channel, which includes cable cords and connecting hardware, shall be 100 ohms for all frequencies between 1 and 100 MHz. The tolerance of the characteristic impedance shall not exceed the nominal impedance by more than 15 ohms over the frequency range 1-100 MHz.

---

1. This equation approximates the insertion loss specification at discrete frequencies for Category 5 100 meter links specified in ANSI/TIA/EIA-568-A Annex E and in TSB-67.

40.8.2.3 Return Loss

In order to limit the amount of echo noise signals at the input to each duplex channel receiver, each link segment duplex channel shall meet the return loss specified below at all frequencies from 1-100 MHz.

40.8.2.3.1 Channel Return Loss

$$\text{Return\_Loss}(f) \begin{cases} I5 & (1\text{-}20\ \text{MHz}) \\ 15\text{-}10\text{Log}(f/20) & (2\text{-}100\ \text{MHz}) \end{cases} \quad (\text{dB})$$

where f is the frequency in MHz.

Note: Return Loss as specified in IEC 11801 meets these specifications.

40.8.3 Coupling Parameters

In order to limit the noise coupled into a duplex channel from adjacent duplex channels, Near-End Crosstalk (NEXT) loss and Equal Level Fair-End Crosstalk (ELFEXT) loss are specified for each link segments. In addition, since each duplex channel can disturbed by more than one duplex channel, Multiple Disturber Near-End Crosstalk (MDNEXT) noise and Multiple Disturber Equal Level Far-End Crosstalk (MDELFEXT) noise are also specified.

40.8.3.1 Differential Near-End Crosstalk (NEXT) Loss

In order to limit the crosstalk noise at the near end of a link segment, the differential pair-to-pair Near-End Crosstalk (NEXT) loss between a duplex channel and the other three duplex channels is specified to meet the symbol error rate specified in ___ and the noise specifications specified in ___. The NEXT loss between all duplex channels of a link segment shall be at least $27.1 - 16.8\text{Log}_{10}(f/100)$[1].

Where: f is the frequency in MHz over the frequency range 1 to 100 MHz.

40.8.3.2 Equal Level Far-End Crosstalk (ELFEXT) Loss

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk noise at the far end of each link segment duplex channel and meet the BER objective specified in ___ and the noise specification in ___. Far-End Crosstalk (FEXT) noise is crosstalk noise that appears at the far end of a duplex channel (disturbed channel) which is coupled from another duplex channel (disturbing channel) with the noise source (transmitters) at the near end. FEXT loss is defined as

FEXT_Loss(f) = 20Log10(Vpds(f)/Vpcn(f))

and ELFEXT_Loss is defined as

ELFEXT_Loss(f) = 20Log10(Vpds(f)/Vpcn(f)) - SLS_Loss(f)

where: Vpds = peak voltage of disturbing signal (near-end transmitter),

1. This equation approximates the NEXT loss specification at discrete frequencies for Category 5 100 meter links specified in ANSI/TIA/EIA-568-A Annex E and in TSB-67.

Vpcn = peak crosstalk noise at far end of disturbed channel,

SLS_Loss = insertion loss of disturbed channel in dB.

To limit the FEXT noise from the adjacent duplex channels, The ELFEXT loss between each duplex channel shall be greater then 19 - $20Log_{10}(f/100)$ dB (where f is the frequency in MHz) over the frequency range 1 to 100 MHz.

40.8.4 Delay

In order to send data over four duplex channels in parallel simultaneously, the propagation delay of each duplex channel as well as the difference in delay between any two of the four channels are specified. This ensures the 1000 Mbps data that is divided across four channels is properly assembled at the far end receiver. This also ensures the round trip delay requirement for effective collision detection is met.

40.8.4.1 Maximum Link Delay

The propagation delay of a link segment shall not exceed 570 ns at all frequencies between 2 MHz and 100 MHz.

40.8.4.2 Link Delay Skew

The difference in propagation delay, or skew, between all duplex channel pair combinations of a link segment, under all conditions, shall not exceed 50 ns at all frequencies from 1 MHz to 100 MHz. It is a further functional requirement that once installed, the skew between any two of the four duplex channels due to environmental conditions shall not vary more than 10 ns, within the above requirement.

40.8.5 Common Mode Tolerance (note: this should probably go into the receiver section)

40.8.6 Noise Environment

The 1000BASE-T link segment noise environment consists primarily of echo signals, multi-disturber NEXT noise, multi-disturber FEXT noise and noise from external sources. Each duplex channel is exposed to this noise. Since each receiver will contain both a NEXT noise canceler and echo canceler it expected the resulting residual noise will be due to FEXT noise and external noise.

40.8.6.1 Echo Noise

In order to achieve simultaneous bi-directional transmission a transmitter and receiver (PMD) are connected to each end of a duplex link segment using a hybrid type network. The impedance mismatches at the PMD-duplex link interface and at other locations in the duplex link segment cause some the transmitted signal energy to be reflected into the receiver, which are referred to as echo noise signals. Controlling the return loss of the duplex link and the trans-hybrid loss of the hybrid will minimize this echo signal. 40.x.x defines the specification for canceling the echo signals.

The Echo Noise on each duplex channel of a link segment should not exceed xx mVp. This assumes the link segment meets the Return Loss specification of 6.2.3.

40.8.6.2 Crosstalk Noise.

40.8.6.2.1 Multiple Disturber Near-End Crosstalk (NEXT) Noise

Since four duplex links, each carrying 250 Mb/s data, are used to provide 1000 Mb/s, the NEXT noise from three near-end duplex channel transmitters will be present at each near-end duplex channel receiver. The NEXT noise canceler specification contained in 40.x.y defines the method for the receiver to cancel the MDNEXT noise signals.

The MDNEXT noise on a duplex channel should not exceed xx mVp.

This specification is compatible with the assumption that:

a) The NEXT loss between all duplex channels of a link segment shall be at least $27.1 - 16.8\text{Log}_{10}(f/100)$[1].

40.8.6.2.2 Multiple Disturber Far-end Crosstalk (FEXT) Noise

Since four duplex links, each carrying 250 Mb/s data, are used to provide 1000 Mb/s, the FEXT noise from three near-end duplex channel transmitters will be present at each far-end duplex channel receiver.

The MDFEXT noise on a duplex channel should not exceed __ mVp.

This specification is compatible with the assumption for each disturbed pair that:

a) One disturbing pair-to-disturbed pair with ELFEXT (Equal Level Far-End Crosstalk) loss shall be at least $19 - 20\text{Log}_{10}(f/100)$ dB.

b) One disturbing pair-to-disturbed pair with ELFEXT (Equal Level Far-End Crosstalk) loss shall be at least $21 - 20\text{Log}_{10}(f/100)$ dB.

c) One disturbing pair-to-disturbed pair with ELFEXT (Equal Level Far-End Crosstalk) loss shall be at least $27 - 20\text{Log}_{10}(f/100)$ dB.

The composite FEXT noise is the noise measured at the output of a filter connected to the output of the far end of a disturbed duplex channel using maximum level 1000BASE-T transmitters attached to the near end of the three disturbing duplex channels.

The filter is a 5th order Butterworth filter with a 3 dB cutoff at 100 MHz.

40.8.6.3 External Coupled Noise

The noise coupled from external sources, measured at the output of a filter connected to the output of the near end of disturbed duplex channel should not exceed xx mV peak.

The filter is a 5th order Butterworth filter with a 3 dB cutoff at 100 MHz.MDI specification

Editor's Note: We may need update to reference latest connectors.

---

1. This equation approximates the NEXT loss specification at discrete frequencies for Category 5 100 meter links specified in ANSI/TIA/EIA-568-A Annex E and in TSB-67.

40.9 MDI specification

This clause defines the MDI. The link topology requires a crossover function between PMAs. Implementation and location of this crossover are also defined in this clause.

40.9.1 MDI connectors

Eight-pin connectors meeting the requirements of section 3 and figures 1-4 of IEC 603-7, Detail Specification for Connectors, 8-Way shall be used as the mechanical interface to the balanced cabling. The plug connector shall be used on the balanced cabling and the jack on the PHY. These connectors are depicted (for informational use only) in figure 40-29 and figure 40-30. The assignment of PMA signals to connector contacts for PHYs is shown in table 40-17.

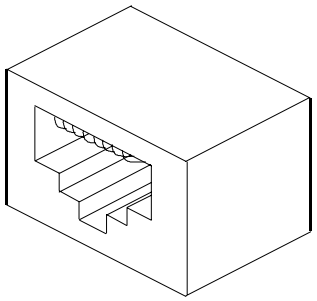


Figure 40-29—MDI connector

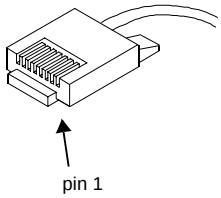


Figure 40-30—Balanced cabling connector

Table 40-17— Assignment of PMA signals to MDI pin-outs

Contact	PHY	MDI labeling requirement
1	BI_DA+	BI_DA+
2	BI_DA-	BI_DA-
3	BI_DB+	BI_DB+
4	BI_DC+	BI_DC+
5	BI_DC-	BI_DC-
6	BI_DB-	BI_DB-
7	BI_DD+	BI_DD+
8	BI_DD-	BI_DD-

40.10 System considerations

The repeater unit specified in clause 41 forms the central unit for interconnecting 1000BASE-T twisted-pair links in networks of more than two nodes. The proper operation of a CSMA/CD network requires that network size be limited to control round-trip propagation delay as specified in clause 42.

When operated in Full Duplex mode where CSMA/CD requirements do not apply, 1000BASE-T balanced cabling links are limited to 100 meters as per ISO/IEC11801.

40.11 Environmental specifications

40.11.1 General safety

All equipment meeting this International Standard shall conform to IEC Publication 950.

40.11.2 Network safety

This clause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cabling systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network.

40.11.2.1 Installation

It is a mandatory functional requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

40.11.2.2 Grounding

Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection.

WARNING—It is assumed that the equipment to which the PHY is attached is properly grounded, and not left floating nor serviced by a “doubly insulated, ac power distribution system.” The use of floating or insulated equipment, and the consequent implications for safety are beyond the scope of this standard.

40.11.2.3 Installation and maintenance guidelines

It is a mandatory functional requirement that, during installation and maintenance of the cabling plant, care be taken to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

40.11.2.4 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 1000BASE-T equipment. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the “battery” and ringing voltages. Although there is no universal standard, the following maximums generally apply.

Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 ohm source impedance.

Ringing voltage is a composite signal consisting of an AC component and a DC component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 ohm source resistance. The DC component is 56 Vdc with a 300 ohm to 600 ohm source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 1000BASE-T equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE—Wiring errors may impose telephony voltages differentially across 1000BASE-T transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, receivers will generally appear to the telephone system as off-hook telephones. Therefore, full-ring voltages will be applied for only short periods. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to the low resistance of the transformer coil.

40.11.3 Environment

40.11.3.1 Electromagnetic emission

The twisted-pair link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

40.11.3.2 Temperature and humidity

The twisted-pair link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

40.11.4 Cabling specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801.

40.12 PHY labeling

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Data rate capability in Mb/s.
b) Power level in terms of maximum current drain (for external PHYs).
c) Port type (i.e., 1000BASE-T)
d) Any applicable safety warnings.

40.13 Delay constraints

Proper operation of a CSMA/CD LAN, operating in half duplex mode, demands that there be an upper bound on the propagation delays through the network. This implies that MAC, PHY and repeater implementors must conform to certain delay minima and maxima, and that network planners and administrators conform to constraints regarding the cabling topology and concatenation of devices. MAC constraints are contained in clause ****. Topological constraints are contained in clause 42. In the full duplex mode of operation, DTEs are not required to conform to the constraints specified in this section.

The reference point for all MDI measurements is the peak point of the mid-cell transition corresponding to the reference code-bit, as measured at the MDI.

40.13.1 PHY delay constraints (exposed GMII)

Every 1000BASE-T PHY with an exposed GMII shall comply with the bit delay constraints specified in table 40-18. These figures apply for all 1000BASE-T PMDs.

Table 40-18— MDI to MII delay constraints (exposed GMII) ****REVISE

Sublayer Measurement Points	Event	Min (bits)	Max (bits)	Input Timing Reference	Output Timing Reference
MII ⇔ MDI	TX_EN Sampled to MDI Output	7	9	TX_CLK rising	1st symbol of SSD
	MDI input to CRS assert		25	1st symbol of SSD	
	MDI input to CRS de-assert		29	1st ONE	
	MDI input to COL assert		25	1st symbol of SSD	
	MDI input to COL de-assert		29	1st symbol of SSD	
	TX_EN sampled to CRS assert	0	4	TX_CLK rising	
	TX_EN sampled to CRS de-assert	0	16	TX_CLK rising	

Editor's Note: Delay constraints not yet updated.--CKM

40.13.2 DTE delay constraints (unexposed GMII)

Every 1000BASE-T DTE with no exposed GMII shall comply with the bit delay constraints specified in table 40-19. These figures apply for all 1000BASE-T PMDs.

Table 40-19— DTE delay constraints (unexposed GMII)**REVISE**

Sublayer Measurement Points	Event	Min (bits)	Max (bits)	Input Timing Reference	Output Timing Reference
MAC ⇔ MDI	MAC transmit start to MDI output		13		1st symbol of SSD
	MDI input to MDI output (worst case non-deferred transmit)		50	1st symbol of SSD	1st Symbol of SSD
	MDI input to collision detect		33	1st symbol of SSD	
	MDI input to MDI output = Jam (worst case collision response)		50	1st symbol of SSD	1st symbol of SSD

Editor's Note: Delay constraints not yet updated.--CKM

40.14 Protocol implementation conformance statement (PICS) proforma for clause 40, physical coding sublayer (PCS), physical medium attachment sublayer (PMA) and baseband medium, type 1000BASE-T

The supplier of a protocol implementation that is claimed to conform to IEEE 802.3ab physical coding sublayer (PCS) or physical medium attachment sublayer (PMA) type 1000BASE-T complete the following Protocol Implementation Conformance Statement (PICS) proforma.

Instructions for interpreting and filling out the PICS proforma may be found in clause 21.

Permission is hereby granted for users of this International Standard to reproduce this PICS Proforma subclause for any purpose.

40.14.1 Identification

40.14.1.1 Implementation identification

Supplier	
Contact point for queries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification - e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE—(1) Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE—(2) The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

40.14.1.2 Protocol summary

Identification of protocol specification	IEEE Std 802.3ab-1998 Physical coding sublayer (PCS), physical medium attachment sublayer (PMA) and baseband medium, type 1000BASE-T
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exceptions items been required? No[] Yes[] (See clause 21; The answer Yes means that the implementation does not conform to the standard)	
Date of Statement	

40.14.2 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*GMII	Exposed GMII interface	*****	O	Yes [] No []	Devices supporting this option must also support the PCS option.
PC	PHY Control Functions	40.3	M	Yes []	Required for proper operation of the PHY.
*PCS	PCS Functions	40.4	O	Yes [] No []	Required for integration with DTE or GMII.
*PMA	Exposed PMA service interface	40.5	O	Yes [] No []	Required for integration into symbol level repeater core.
NWY	Support for Auto-Negotiation (clause 28)	40.6	M	Yes []	Required
*INS	Installation / cabling	40.8	O	Yes [] No []	Items marked with INS include installation practices and cabling specifications not applicable to a PHY manufacturer.

40.14.3 PICS pro forma table for compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
CCO1	Compatibility at the MDI	40.1.3.1	M	Yes []	
CCO2	Auto-Negotiation required	40.1.3.4	M	Yes []	
CCO3	State diagrams prevail	40.1.4	M	Yes []	in discrepancy between text and state diagram.

40.14.4 PICs proforma table for the PHY Control function

Item	Feature	Subclause	Status	Support	Value/Comment
PC01	PHY Control shall	40.3.1	M	Yes []	comply with the state diagram descriptions given in figure 40-4.
PC02	PHY Control shall	40.3.2.1.2	M	Yes []	generate PHYC_CONFIG.indicate messages synchronously with every GMII TX_CLK cycle.
PC03	Upon receipt of the PHYC_CONFIG primitive, PCS and PMA Clock Recovery shall	40.3.2.1.3	M	Yes []	perform their functions in master or slave configuration according to the value of the parameter config.
PC04	PCS Transmit function shall	40.3.2.2	M	Yes []	be capable of convolutionally encoding the data stream as per the link partner's decoding ability.
PC05	PHY Control shall	40.3.2.2.2	M	Yes []	generate PHYC_CODING.indicate messages synchronously with every GMII RX_CLK cycle.
PC06	Upon reception of the PHYC_CODING.indicate primitive, the PCS shall	40.3.2.2.3	M	Yes []	perform its encoding functions according to the value assumed by the parameter coding_enable.
PC07	PHY Control shall	40.3.2.2.2	M	Yes []	generate PHYC_TXMODE.indicate messages synchronously with every GMII TX_CLK cycle.
PC08	Upon receipt of the PHYC_TXMODE.indicate primitive, the PCS shall	40.3.2.2.3	M	Yes []	perform its Transmit function as described in 32.3.1.2.
PC9	The PCS shall	40.3.2.4.2	M	Yes []	generate PHYC_RXSTATUS.request messages synchronously with signals received at the MDI.
PC10	The PCS shall	40.3.2.4.2	M	Yes []	prevent that the value of the parameter loc_rcvr_status is modified while TX_EN=1 in order to avoid that a transition from data to idle mode or from idle to data mode occurs while a packet is being presented to the PCS at the GMII.
PC11	The PCS shall	40.3.2.5.2	M	Y []	generate PHYC-REMRXTATUS.request messages synchronously with signals received at the GMII.

Item	Feature	Subclause	Status	Support	Value/Comment
PC12	PCS Transmit shall	40.3.3	M	Y []	send quinary symbols according to the value assumed by tx_mode.
PC13	When tx_mode assumes the value of SEND_N	40.3.3	M	Y []	transmission of sequences of quinary symbols representing an GMII data stream, the idle mode, or control sequences shall take place.
PC14	When tx_mode assumes the value of SEND_I	40.3.3	M	Y []	transmission of sequences of quinary symbols representing the idle mode shall take place.
PC15	When tx_mode assumes the value of SEND_I	40.3.3	M	Y []	transmission of zero symbols shall take place.
PC16	The maxwait_timer shall expire	40.3.3	M	Y []	750 ms after entering the SLAVE DFC CONVERGENCE state.
PC17	The minwait_timer shall expire	40.3.3	M	Y []	128T=1.024 μs after being started.

40.14.5 PICS proforma tables for the Physical Coding Sublayer (PCS)

Item	Feature	Subclause	Status	Support	Value/Comment
PCT01	The PCS shall	40.4.5.2	M	Y []	implement the Transmit process as depicted in figure 40-9 including compliance with the associated state variables specified in 40.4.4
PCT02	PCS Transmit function shall	40.4.1.2	M	Y []	conform to the PCS Transmit state diagram in figure 40-9.
PCT03	If the parameter config provided to the PCS by the PHY Control function via the PHYC_CONFIG.indicate message assumes the value MASTER, PCS Transmit shall	40.4.1.2.1	M	Y []	employ the transmitter side-stream scrambler generator polynomial specified for use with MASTER in 40.4.1.2.1.
PCT04	If the parameter config provided to the PCS by the PHY Control function via the PHYC_CONFIG.indicate message assumes the value SLAVE, PCS Transmit shall	40.4.1.2.1	M	Y []	employ the transmitter side-stream scrambler generator polynomial specified for use with SLAVE in 40.4.1.2.1.
PCT05	Transmission of quinary symbol pairs over wire pairs	40.4.1.2	M	Y []	Symbols A_n, B_n, C_n and D_n are transmitted over BI_DA, BI_DB, BI_DC and BI_DD respectively.
PCT06	If tx_error_n=1 is asserted when the condition (tx_enable_n * tx_enable_{n-2}) = 1, where "*" denotes the logic AND operator, error indication is signaled by means of symbol substitution, the values of Sd_n[5:0] shall be	40.4.1.2.5	M	Y []	ignored by PCS Transmit and the symbols corresponding to the row denoted as "Xmt_Err" in table 40-1 and table 40-2 shall be used.
PCT07	If tx_error_n=0 is asserted when the variable $csreset_n$ = 1, the convolutional encoder reset condition is normal. This condition is indicated by means of symbol substitution, where the values of Sd_n[5:0] are ignored by PCS Transmit and the symbols corresponding to the row denoted as "CSReset" in table 40-1 and table 40-2 shall be used.	40.4.1.2.5	M	Y []	

Item	Feature	Subclause	Status	Support	Value/Comment
PCT08	If tx_error_n=1 is asserted when the variable $csreset_n$ = 1, the convolutional encoder reset condition must indicate carrier extension. In this condition, the values of Sd_n[5:0] are ignored by PCS Transmit and the symbols corresponding to the row denoted as "CSExtend" in table 40-1 and table 40-2 shall be used when TxD_n = 0x'0F, and the row denoted as "CSExtend_Err" in table 40-1 and table 40-2 shall be used when TxD_n = 0x'1F. The latter condition denotes Carrier Extension with Error. In case Carrier Extension with Error is indicated during the first byte of csreset, the Error condition shall be encoded during the second byte of csreset, and during the subsequent two bytes of the End-of-Stream delimiter as well.	40.4.1.2.5	M	Y []	
PCT09	The symbols corresponding to the SSD1 row in table 40-1 shall be used when the condition (tx_enable_n) * (! tx_enable_{n-1}) = 1.	40.4.1.2.5	M	Y []	
PCT10	The symbols corresponding to the SSD2 row in table 40-1 shall be used when the condition (tx_enable_{n-1})*(! tx_enable_{n-2}) = 1.	40.4.1.2.5	M	Y []	
PCT11	If Carrier Extend Error is indicated during ESD, that is, when tx_error_n = 1 and Tx_D_n = 0x'1F, the symbols corresponding to the ESD_Ext_Err row in table 40-1 shall be used.	40.4.1.2.5	M	Y []	
PCT12	The symbols corresponding to the ESD1 row in table 40-1 shall be used when the condition (!tx_enable_{n-2}) * (tx_enable_{n-3}) = 1, in the absence of Carrier Extend Error indication at time n.	40.4.1.2.5	M	Y []	

Item	Feature	Subclause	Status	Support	Value/Comment
PCT13	The symbols corresponding to the ESD2_Ext_0 row in table 40-1 shall be used when the condition (!tx_enable_{n-3}) * (tx_enable_{n-4}) * (!tx_error_{n}) * (!tx_error_{n-1}) = 1.	40.4.1.2.5	M	Y []	
PCT14	The symbols corresponding to the ESD2_Ext_1 row in table 40-1 shall be used when the condition (!tx_enable_{n-3}) * (tx_enable_{n-4}) * (!tx_error_{n}) * (tx_error_{n-1}) = 1.	40.4.1.2.5	M	Y []	
PCT15	The symbols corresponding to the ESD2_Ext_2 row in table 40-1 shall be used when the condition (!tx_enable_{n-3}) * (tx_enable_{n-4}) * (tx_error_{n}) * (tx_error_{n-1}) = 1, in the absence of Carrier Extend Error indication.	40.4.1.2.5	M	Y []	

40.14.5.1 PCS receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR01	PCS Receive function shall	40.4.1.3	M	Y []	conform to the PCS Receive state diagram shown in figure 40-10
PCR02	The PCS shall	40.4.5.3	M	Y []	implement the Receive process as depicted in figure 40-10, including compliance with the associated state variables as specified in 40.4.4.
PCR03	For side-stream descrambling, the MASTER PHY shall employ	40.4.1.3.1	M	Y []	the receiver scramber generator polynomial specified for MASTER operation in 40.4.1.3.1.
PCR04	For side-stream descrambling, the SLAVE PHY shall employ	40.4.1.3.1	M	Y []	the receiver scrambler generator polynomial specified for SLAVE operation in 40.4.1.3.1.

40.14.5.2 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	The PCS Reset function shall	40.4.1.1	M	Y []	be executed any time “power on”, receipt of a request for reset from the management entity, or receipt of a request for reset from the PHY Control occur.
PCO2	THE PCS shall	40.4.1.2.1	M	Y []	employ the appropriate side-stream scrambler shown in 40.4.1.2.1, as determined by the value (MASTER/SLAVE) assumed by the PHY.
PCO3	The PCS shall	40.4.5.4	M	Y []	implement the Carrier Sense process as depicted in figure 40-11, including compliance with the associated state variables as specified in 40.4.4.
PCO4	PCS Carrier Sense function shall	40.4.1.4	M	Y []	comply with the PCS Carrier Sense state diagram shown in figure 40-11 including compliance with the associated state variables specified in 40.4.4.
PCO5	GMII COL signal shall be asserted while	40.4.1.5	M	Y []	a PCS collision is being detected.
PCO6	The GMII signal COL shall remain de-asserted.	40.4.1.5	M	Y []	a PCS collision is not being detected.
PCO7	No spurious PCS management entity signals shall be emitted onto the MDI while the PHY is held in power down mode as defined in 22.2.4.1.5, independently of the value of TX_EN, or when released from power down mode, or when power is first applied to the PHY.	40.4.2.2	M	Y []	
PCO8	Frames passed from the PCS to the PMA sublayer shall	40.4.3	M	Y []	have the structure shown in figure 40-7.
PC09	The PCS shall	40.4.5.2			implement the Data Transmission Enabling process as depicted in figure 40-8 including compliance with the associated state variables as specified in 40.4.4.
PCO10	TX_CLK shall be generated	40.4.4.2	M	Y []	Synchronously with symb_timer with tolerance as specified in ****.

40.14.6 PICS proforma tables for the Physical Medium Attachment (PMA)

Item	Feature	Subclause	Status	Support	Value/Comment
PMF1	PMA Reset function shall be executed	40.5.1.1.1	M	Y []	at power on and upon receipt of a reset request from the management entity.
PMF2	PMA transmit shall transmit	40.4.1.2	M	Y []	symbols A_n, B_n, C_n, D_n over wire pairs BI-DA, BI_DB, BI_DC and BI_DD respectively.
PMF3	PMA Transmit shall	40.5.1.1.2	M	Y []	continuously transmit onto the MDI pulses modulated by the quinary symbols given by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC] and tx_symb_vector[BI_DD], respectively.
PMF4	The four transmitters shall be driven by the same transmit clock.	40.5.1.1.2	M	Y []	
PMF5	PMA Transmit function will	40.5.1.1.2	M	Y []	follow the mathematical description given in 40.5.1.2.1.
PMF6	PMA Transmit shall comply with	40.5.1.1.2	M	Y []	the electrical specifications given in 40.7.
PMF7	PMA Receive function shall	40.5.1.1.3	M	Y []	translate the signals received on pairs BI_DA BI_DB, BI_DC and BI_DD into the PMA_UNITDATA.indicate parameter rx_symb_vector with a symbol error rate of less than one part in 10^{10}.
PMF8	The Link Monitor function shall	40.5.1.1.4	M	Y []	comply with the state diagram shown in figure 40-13.
PMF9	Clock Recovery function shall provide	40.5.1.1.5	M	Y []	a clock suitable for synchronous signal sampling on each line so that the symbol-error rate indicated in 40.5.1.1.3 is achieved.
PMF10	The symbol response shall comply with	40.5.1.2.1	M	Y []	the electrical specifications given in 40.7.
PMF11	The four signals received on pairs BI_DA, BI_DB, BI_DC and BI_DD shall be processed within the PMA Receive function to yield	40.5.1.2.2	M	Y []	the quinary received symbols rx_symb_vector[BI_DA], rx_symb_vector[BI_DB], rx_symb_vector[BI_DC] and rx_symb_vector[BI_DD]. .

40.14.6.1 PMA service interface

Item	Feature	Subclause	Status	Support	Value/Comment
PMS1	Continuous generation of PMA_TYPE	40.5.2.1.2	M	Y []	
PMS2	The PMA shall generate	40.5.2.5.2	M	Y []	PMA_LINK.indicate to indicate the value of link_status.
PMS3	Effect of receipt of PMA_LINK.request messages	40.5.2.4.3	M	Y []	while link_control=SCAN_FOR_CARRIER or link_control=DISABLE, the PMA shall report link_status=fail; while link_control=ENABLE, PHY determines operations to be performed by the PHY.

40.14.7 PICS proforma tables for management functions

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	A 1000BASE-T PHY shall	40.6	M	Y []	provide equivalents to MII registers 9 and 10 for its control and status functions.
MF2	On power-up the Auto-Negotiation advertisement register shall	40.6.1.1	M	Y []	have the configuration specified in 40.6.1.1
MF3	Bits U0-U6 of Next Page 1 shall	40.6.1.1	M	Y []	be copied from GMII register 9:12-6.
MF4	Bits U0-U10 of Next Page 2 shall	40.6.1.1	M	Y []	shall be used to define the seed bits for the MASTER-SLAVE negotiation process as defined in 40.6.1.1
MF5	A 1000BASE-T PHY shall	40.6.3	M	Y []	used register addresses 9 and 10 for its control and status functions.
MF6	Register 9 shall	40.6.3.1	M	Y []	provide values as specified in table 40-6.
MF7	A PHY with 1000BASE-T capability shall	40.6.3.1.1	M	Y []	be placed in transmitter test mode 1 when bit 9:15 is set to logic zero, bit 9:14 is set to logic zero and bit 9:13 is set to logic one.
MF8	A PHY with 1000BASE-T capability shall	40.6.3.1.1	M	Y []	be placed in transmitter test mode 2 when bit 9:15 is set to logic zero, bit 9:14 is set to logic one and bit 9:13 is set to logic zero.
MF9	A PHY with 1000BASE-T capability shall	40.6.3.1.1	M	Y []	be placed in transmitter test mode 3 when bit 9:15 is set to logic zero, bit 9:14 is set to logic one and bit 9:13 is set to logic one.
MF10	A PHY with 1000BASE-T capability shall	40.6.3.1.1	M	Y []	be placed in transmitter test mode 4 when bit 9:15 is set to logic one, bit 9:14 is set to logic zero and bit 9:13 is set to logic zero.
MF11	MASTER-SLAVE configuration negotiation will determine PHY configuration if	40.6.3.1.2	M	Y []	bit 9.12 is set to logic zero.
MF12	Manual MASTER-SLAVE configuration will be set manually using bit 9:11 to set the value if	40.6.3.1.2	M	Y []	bit 9.12 is set to logic one.
MF13	Bit 9:11 shall be used to report the results of manual MASTER-SLAVE configuration.	40.6.3.1.3	M	Y []	

Item	Feature	Subclause	Status	Support	Value/Comment
MF14	Bit 9:10 shall	40.6.3.1.4	M	Y []	be set to logic zero if the PHY is a DTE device and be set to logic one if the PHY is a repeater device port.
MF15	Bit 9:9 shall	40.6.3.1.5	M	Y []	be used to indicate the full-duplex ability that will be advertised to the link partner.
MF16	Bit 9:8 shall	40.6.3.1.6	M	Y []	be used to indicate the half-duplex ability that will be advertised to the link partner.
MF17	Bit 9:7 shall	40.6.3.1.7	M	Y []	be used to determine what the link partner should use for its coding method.
MF18	Bit 9:6 shall	40.6.3.1.8	M	Y []	be used to determine the value for the asymmetric pause direction bit.
MF19	Bits 9:5:0 shall	40.6.3.1.9	M	Y []	be set to logic zero.
MF20	Bits 9.9:0 shall be ignored when read	40.6.3.1.9	M	Y []	
MF21	A PHY shall return a value of zero for bits 9.9:0.	40.6.3.1.9	M	Y []	
MF22	Register 10 shall	40.6.3.2	M	Y []	be used as shown in table 40-7.
MF23	The MASTER-SLAVE Manual Configuration Fault bit shall be implemented	40.6.3.2.1	M	Y []	with a latching function, such that the occurrence of a MASTER-SLAVE Manual Configuration Fault will cause the MASTER-SLAVE Manual Configuration Fault bit to be set and remain set until cleared.
MF24	The MASTER-SLAVE Manual Configuration Fault bit shall be cleared	40.6.3.2.1	M	Y []	each time register 10 is read by the management interface.
MF25	The MASTER-SLAVE Management Configuration Fault bit shall also be cleared by	40.6.3.2.1	M	Y []	a 1000BASE-T PMA reset.

40.14.7.1 100BASE-T2 Specific Auto-Negotiation Requirements

AN1	Base Page shall be followed with	40.6.1.1	M	Y []	a Next Page with a message code containing the 1000BASE-T Technology Ability Message Code (9).
AN2	Message Next Page shall be followed with	40.6.3.2.1	M	Y []	two Unformatted Message Next Pages containing the 1000BASE-T Technology Ability fields as described in table 40-8.
AN3	MASTER-SLAVE relationship shall be determined by	40.6.3.5	M	Y []	using table 40-9 with the 1000BASE-T Technology Ability Next Page bit values specified in table 40-8.
AN4	Successful completion of MASTER-SLAVE resolution shall	40.6.3.5	M	Y []	be treated as MASTER-SLACE configuration resolution complete and the 1000BASE-T Status Register bit 10:14 shall be set to logical one.
AN5	Upon successful completion of MASTER-SLAVE resolution shall	40.6.3.5	M	Y []	the 1000BASE-T Status Register bit 10:14 shall be set to logical one.
AN6	A seed counter shall be provided to	40.6.3.5	M	Y []	track the generation of seeds.
AN7	At start-up, the seed counter shall be set to	40.6.3.5	M	Y []	zero.
AN8	The seed counter shall be incremented	40.6.3.5	M	Y []	every time a new random seed is sent.
AN9	Maximum seed attempts before declaring a MASTER_SLAVE configuration Resolution Fault	40.6.3.5	M	Y []	seven.
AN10	During MASTER_SLAVE configuration, the device with the lower seed value shall	40.6.3.5	M	Y []	become the SLAVE.
AN11	Both PHYs set in manual mode to be either MASTER or SLAVE shall be treated as	40.6.3.5	M	Y []	MASTER-SLAVE resolution fault (Failure) condition
AN12	MASTER-SLAVE resolution fault (failure) condition shall result in	40.6.3.5	M	Y []	MASTER-SLAVE Configuration Resolution Fault bit (10.15) to be set to logical one.
AN13	MASTER-SLAVE Configuration resolution fault condition shall be treated as	40.6.3.5	M	Y []	MASTER-SLAVE Configuration Resolution complete.
AN14	MASTER-SLAVE Configuration resolution fault condition shall cause	40.6.3.5	M	Y []	cause status register bit 10:14 to be set to logical one.
AN15	MASTER-SLAVE Configuration resolution fault condition shall	40.6.3.5	M	Y []	cause link_status_1000BASE-T to be set to FAIL.
AN16	MASTER-SLAVE Configuration resolution fault condition shall	40.6.3.5	M	Y []	force Auto-Negotiation to restart after the link_fail_inhibit_timer has expired.

40.14.8 PICS proforma tables for PMA electrical specifications

Item	Feature	Subclause	Status	Support	Value/Comment
PME1	The value of all components in test circuits shall be accurate to within	40.7	M	Y []	±1%.
PME2	The PHY shall provide electrical isolation between	40.7.1.1	M	Y []	the DTE or repeater circuits including frame ground, and all MDI leads.
PME3	PHY-provided electrical separation shall withstand at least one of three electrical strength tests	40.7.1.1	M	Y []	a) 1500 V rms at 50Hz to 60Hz for 60 s, applied as specified in section 5.3.2 of IEC Publication 950. b) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC Publication 950. c) a sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 µs. (1.2 µs virtual front time, 50 µs virtual time or half value), as defined in IEC Publication 950.
PME4	There shall be no insulation breakdown as defined in Section 5.3.2 of IEC publication 950, during the test.	40.7.1.1	M	Y []	
PME5	The resistance after the test shall be at least	40.7.1.1	M	Y []	2 Megaohms, measured at 500 Vdc.
PME6	The transmitter MASTER/SLAVE timing jitter test channel shall	40.7.1.1.1	M	Y []	be constructed by combining 100 ohm and 120 ohm cable segments that meet or exceed ISO.IEC 11801 category 5 specifications for each pair as shown in figure 40-16 with the lengths and additional restrictions on parameters described in table 40-11.
PME7	The ends of the MASTER/SLAVE timing jitter test channel shall	40.7.1.1.1	M	Y []	be connectorized with connectors meeting or exceeding ISO/IEC 11801 category 5 specifications.
PME8	The return loss of the MASTER/SLAVE timing jitter test channel shall	40.7.1.1.1	M	Y []	meet the return loss requirements of 40.8.2.3.
PME9	The return loss of the MASTER/SLAVE timing jitter test channel shall	40.7.1.1.1	M	Y []	meet the crosstalk requirements of 40.8.3 on each pair.

Item	Feature	Subclause	Status	Support	Value/Comment
PME10	The test modes described in 40.7.1.1.2 shall be provided for testing of the transmitted waveform, transmitter distortion and transmitted jitter.	40.7.1.1.2	M	Y []	
PME11	For a PHY with a GMII interface the test modes shall be enabled by	40.7.1.1.2	M	Y []	setting bits 9:13-15 (1000BASE-T Control Register) of the GMII Management register set as shown in table 40-12.
PME12	The test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal operation.	40.7.1.1.2	M	Y []	
PME13	A PHY without a GMII shall provide a means to provide the test mode functions.	40.7.1.1.2	M	Y []	
PME14	Vendors shall provide a means to enable test modes for conformance testing.	40.7.1.1.2	M	Y []	
PME15	When transmit test mode 1 is enabled, the PHY shall transmit	40.7.1.1.2	M	Y []	the sequence of data symbols specified in 40.7.1.1.2 continuously from all four transmitters.
PME16	When in test mode 1, the transmitter shall time the transmitted symbols	40.7.1.1.2	M	Y []	from a 125.000 MHz $\pm$ 0.01% clock.
PME17	When test mode 2 is enabled, the PHY shall transmit	40.7.1.1.2	M	Y []	the data symbol sequence {+2,-2} repeatedly on all four channels.
PME18	When in test mode 2, the transmitter shall time the transmitted symbols	40.7.1.1.2	M	Y []	from a 25.000 MHz $\pm$ 0.01% clock.
PME19	When transmit test mode 3 is enabled, the PHY shall transmit	40.7.1.1.2	M	Y []	the data symbol sequence {+2,-2} repeatedly on all four channels.
PME20	When in test mode 3, the transmitter shall time the transmitted symbols	40.7.1.1.2	M	Y []	from a 125.000 MHz $\pm$ 0.01% clock.
PME21	When test mode 4 is enabled, the PHY shall transmit	40.7.1.1.2	M	Y []	the data symbols generated by the scrambler polynomial specified in 40.7.1.1.2.

Item	Feature	Subclause	Status	Support	Value/Comment
PME22	When test mode 4 is enabled, the PHY shall	40.7.1.1.2	M	Y []	use the bit sequences generated by the scrambler bits shown in 40.7.1.1.2 to generate the quinary symbols s_n as shown in table 40-13.
PME23	When in test mode 4, the transmitter shall time the transmitted symbols	40.7.1.1.2	M	Y []	from a 125.000 MHz ± 0.01% clock.
PME24	The test fixtures defined in figure 40-20, figure 40-21, figure 40-22 and figure 40-23 or their functional equivalents shall be used for measuring transmitter specifications.	40.7.1.1.3	M	Y []	
PME25	The test filter used in transmitter test fixtures 1 and 3 shall	40.7.1.1.3	M	Y []	have the continuous time transfer function specified in 40.7.1.1.3 or its discrete time equivalent.
PME26	The disturbing signal V_d shall	40.7.1.1.3	M	Y []	have the characteristics listed in table 40-14.
PME27	To allow for measurement of transmitted jitter in master and slave modes the PHY shall provide access to the 125 MHz symbol clock, TX-TCLK that times the transmitted symbols.	40.7.1.1.3	M	Y []	
PME28	To allow for measurement of transmitted jitter in master and slave modes the PHY shall provide a means to enable the TX-TCLK output if it is not normally enabled.	40.7.1.1.3	M	Y []	have the characteristics listed in table 40-14.
PME29	The PMA shall	40.7.1.2	M	Y []	provide the Transmit function specified in 40.4.1.2 in accordance with the electrical specifications of this clause.
PME30	Where a load is not specified, the transmitter shall	40.7.1.2	M	Y []	meet the requirements of clause 40 with a 100 ohm resistive differential load connected to each transmitter output.
PME31	The tolerance on the poles of the test filters used in 40.7 shall be ± 1%.	40.7.1.2	M	Y []	
PME32	When in transmit test mode 1 and observing the differential signal output at the MDI using test fixture 1, for each pair, with no intervening cable, the absolute value of the peak of the waveform at points A and B as defined in figure 40-17 shall fall within	40.7.1.2.1	M	Y []	the range of 0.67 V to 0.82 V (0.75 V ± 0.83 dB).

Item	Feature	Subclause	Status	Support	Value/Comment
PME33	The absolute value of the peak of the waveforms at points A and B shall	40.7.1.2.1	M	Y []	differ by less than 1%.
PME34	The absolute value of the peak of the waveform at points C and D as defined in figure 40-17 shall differ	40.7.1.2.1	M	Y []	from 0.5 times the average of the absolute values of the peaks of the waveform at points A and B by less than 2%.
PME35	When in transmit test mode 1 and observing the differential transmitted output at the MDI, for either pair, with no intervening cabling, the peak value of the waveform at point F as defined in figure 40-17 shall be	40.7.1.2.2	M	Y []	be greater than 73.1% of the magnitude of the negative peak value of the waveform at point F. Point G is defined as the point exactly 500 ns after point F. Point F is defined as the point where the waveform reaches it's minimum value at the location indicated in figure 40-17.
PME36	When in transmit test mode 1 and observing the differential transmitted output at the MDI, for either pair, with no intervening cabling, the peak value of the waveform at point J as defined in figure 40-17 shall be	40.7.1.2.2	M	Y []	be greater than 73.1% of the magnitude of the peak value of the waveform at point H. Point J is defined as the point exactly 500 ns after point H. Point H is defined as the point where the waveform reaches it's maximum value at the location indicated in figure 40-17.
PME37	When in test mode 1 and observing the differential signal output at the MDI using transmitter test fixture 1, for each pair, with no intervening cable, the voltage waveforms at points A, B, C, D defined in figure 40-17, after the normalization described below, shall	40.7.1.2.3	M	Y []	lie within the time domain template 1 defined in figure 40-24 and the piecewise linear interpolation between the points in table 40-15. The waveforms may be shifted in time as appropriate to fit within the template.
PME38	When in test mode 1 and observing the differential signal output at the MDI using transmitter test fixture 1, for each pair, with no intervening cable, the voltage waveforms at points F and H defined in figure 40-17, after the normalization described below, shall	40.7.1.2.3	M	Y []	lie within the time domain template 2 defined in figure 40-24 and the piecewise linear interpolation between the points in table 40-16. The waveforms may be shifted in time as appropriate to fit within the template.
PME39	The time span of the waveforms so processed shall be	40.7.1.2.4	M	Y []	be less than 10 millivolts.

Item	Feature	Subclause	Status	Support	Value/Comment
PME40	When in test mode 2 or test mode 3, the peak-to-peak jitter of the zero crossings of the differential signal output at the MDI relative to the corresponding edge of TX-TCLK shall	40.7.1.2.5	M	Y []	be less than 0.100 ns for each transmitter. The corresponding edge of TX-TCLK is the edge of the transmit test clock, in polarity and time, that generates the zero-crossing transition being measured.
PME41	When in the normal mode of operation as the master, receiving valid signal from a compliant PHY operating as the slave using the test channel defined in 40.7.1.1.1, with test channel port B connected to the slave, the peak-to-peak value of the slave TX-TCLK jitter relative to the master TX-TCLK shall	40.7.1.2.5	M	Y []	be less than 2.4 ns after the receiver is properly receiving the data and has set bit TBD of the GMII management register set to 1.
PME42	When the jitter waveform on TX_TCLK is filtered by a high pass filter, $H_{jf1}(f)$ having the transfer function specified in 40.7.1.2.5, the peak-to-peak value of the resulting filtered timing jitter shall	40.7.1.2.5	M	Y []	be less than 0.250 ns.
PME43	When in the normal mode of operation as the slave, receiving valid signal from a compliant PHY operating as the master using the test channel defined in 40.7.1.1.1, with test channel port A connected to the slave, the peak-to-peak value of the master TX-TCLK jitter relative to an unjittered reference shall	40.7.1.2.5	M	Y []	be less than 2.4 ns after the receiver is properly receiving the data and has set bit TBD of the GMII management register set to 1.
PME44	When the jitter waveform on TX_TCLK is filtered by a high pass filter, $H_{jf2}(f)$, having the transfer function below, the peak-to-peak value of the resulting filtered timing jitter shall	40.7.1.2.5	M	Y []	be less than 0.250 ns greater than the simultaneously measured peak-to-peak value of the master jitter filtered by $H_{jf1}(f)$.
PME45	For all jitter measurements the peak-to-peak value shall be	40.7.1.2.5	M	Y []	measured over an unbiased sample of 10^{10} clock edges.
PME46	The quinary symbol transmission rate on each pair shall be	40.7.1.2.6	M	Y []	125.000 MHz ± 0.01%

Item	Feature	Subclause	Status	Support	Value/Comment
PME47	The PMA shall provide the Receive function specified in 40.4.1.3 in accordance with the electrical specifications of this clause	40.7.1.3	M	Y []	
PME48	The patch cabling and interconnecting hardware used in test configurations shall meet or exceed IS).IEC 11801 category 5 specifications.	40.7.1.3	M	Y []	
PME49	Differential signals received on the receive inputs that were transmitted within the specifications given in 40.7.1.2 and have then passed through a link compatible with Clause 40, shall be translated into	40.7.1.3.1	M	Y []	one of the PMA_UNITDATA.indicate messages with a 4-D symbol rate error less than 10^{-10} and sent to the PCS after link bring-up. Since the 4-D symbols are not accessible, this specification shall be satisfied by a packet error rate less than 10^{-7} for 1000 byte packets.
PME50	The receive feature shall	40.7.1.3.2	M	Y []	properly receive incoming data with a 5-level symbol rate within the range 125,000 MHz ± 0.01%.
PME51	While receiving packets from a compliant 1000BASE-T transmitter connected to all MDI pins, a receiver shall send the	40.7.1.3.3	M	Y []	proper PMA_UNITDATA.indicate messages to the PCS for any differential input signal E_s that results in a signal E_{dif} that meets 40.7.1.3.1 even in the presence of common mode voltages E_{cm} (applied as shown in figure 40-25).
PME52	E_{cm} shall be	40.7.1.3.3	M	Y []	a 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%-80%), connected to each of the pairs.
PME53	The differential impedance as measured at the MDI for each transmit/receive channel shall be such that	40.7.1.4.1	M	Y []	any reflection due to differential signals incident upon the MDI from a balanced cabling having an impedance of 100 ohms is at least 17 dB below the incident signal, over the frequency range of 2.0 MHz to 31.25 MHz and at least $12.9 - 20\log_{10}(f/50)$ dB over the frequency range 31.25 MHz to 125 MHz (f in MHz).
PME54	This return loss shall be maintained	40.7.1.4.1	M	Y []	at all times when the PHY is transmitting data.

Item	Feature	Subclause	Status	Support	Value/Comment
PME55	The common-mode to differential-mode impedance balance of each transmit output shall exceed	40.7.1.4.2	M	Y []	the value specified by the equations specified in 40.7.1.4.2. Test mode 4 may be used to generate an appropriate transmitter output.
PME56	Transmitters and receivers shall	40.7.1.4.4	M	Y []	withstand without damage the application of short circuits across any MDI port for an indefinite period of time without damage.
PME57	Transmitters and receivers shall resume	40.7.1.4.4	M	Y []	normal operation after such faults are removed.
PME58	The magnitude of the current through the short circuit specified in PME54 shall not exceed	40.7.1.4.4	M	Y []	300 mA.
PME59	Transmitters shall withstand without damage	40.7.1.4.4	M	Y []	a 1000 V common mode impulse of either polarity (E_{cm} as indicated in figure 40-28).
PME60	The shape of the impulse shall be	40.7.1.4.4	M	Y []	0.3/50 µs (300 ns virtual front time, 50 µs virtual time of half value), as defined in IEC Publication 60.

40.14.9 PICS proforma tables for characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LKS1	1000BASE-T links shall	40.8.1	M	Y []	consist of Category 5 components as specified in ISO/IEC 11801:1995.
LKS2	Unless otherwise specified, link segment testing shall be conducted using	40.8.2	M	Y []	source and load impedances of 100 ohms.
LKS3	The tolerance on the poles of the test filter used in this section shall be	40.8.2		Y []	± 1%.
LKS4	The insertion loss of each duplex channel shall be	40.8.2.1	M	Y []	less than $2.1\ f^{0.529} + 0.4/f$ (dB) at all frequencies from 1 to 100 MHz. This includes the attenuation of the balanced cabling pairs, connector losses, and patch cord losses of the duplex channel.
LKS5	The insertion loss specification shall be met when	40.8.2.1	M	Y []	the duplex channel is terminated in 100 ohms.
LKS6	The nominal differential impedance of each link segment duplex channel, which includes cable cords and connecting hardware, shall be	40.8.2.2	M	Y []	100 ohms at all frequencies between 1 and 100 MHz.
LKS7	The tolerance of the characteristic impedance shall not	40.8.2.2	M	Y []	exceed the nominal impedance by more than 15 ohms over the frequency range 1-100 MHz.
LKS8	Each link segment duplex channel shall	40.8.2.3	M	Y []	meet the return loss specified in 40.8.2.3.1 at all frequencies from 1-100 MHz.
LKS9	The NEXT loss between all duplex channels of a link segment shall be	40.8.3.1	M	Y []	at least $27.1 - 16.8\log_{10}(f/100)$ (where f is the frequency in MHz over the frequency range 1-100 MHz.)
LKS10	The ELFEXT loss between each duplex channel shall be	40.8.3.2	M	Y []	greater than $19 - 20\log_{10}(f/100)$ (where f is the frequency in MHz over the frequency range 1-100 MHz.)
LKS11	The propagation delay of a link segment shall	40.8.4.1	M	Y []	not exceed 50 ns at all frequencies from 1-100 MHz.
LKS12	The difference in propagation delay, or skew, between all duplex channel pair combinations of a link segment under all conditions shall not exceed	40.8.4.2	M	Y []	50 ns at all frequencies between 1 MHz and 100 MHz.

Item	Feature	Subclause	Status	Support	Value/Comment
LKS13	Once installed, the skew between pairs due to environmental conditions shall not vary	40.8.4.2	M	Y []	more than ± 10 ns.
LKS14	The MDNEXT noise on a duplex channels should not exceed	40.8.6.2.1	M	Y []	xx mVp.
LKS15	The measurement specified in LKS14 is compatible with the assumption that the NEXT loss between all duplex channels of a link segment shall be	40.8.6.2.1	M	Y []	at least 27.1 - 16.8$\log_{10}(f/100)$.
LKS16	The MDFEXT noise on a duplex channel should not exceed	40.8.6.2.2	M	Y []	xx mVp
LKS17	The measurement specified in LKS16 is compatible with the assumption that for each disturbed pair one disturbing pair-to-disturbed pair with ELFEXT (Equal Level Far-End Crosstalk) loss shall be	40.8.6.2.2	M	Y []	at least 19 - 20$\log_{10}(f/100)$ dB.
LKS18	The measurement specified in LKS16 is compatible with the assumption that for each disturbed pair one disturbing pair-to-disturbed pair with ELFEXT (Equal Level Far-End Crosstalk) loss shall be	40.8.6.2.2	M	Y []	at least 21 - 20$\log_{10}(f/100)$ dB.
LKS19	The measurement specified in LKS16 is compatible with the assumption that for each disturbed pair one disturbing pair-to-disturbed pair with ELFEXT (Equal Level Far-End Crosstalk) loss shall be	40.8.6.2.2	M	Y []	at least 27 - 20$\log_{10}(f/100)$ dB.
LKS20	The noise coupled from external sources, measured at the output of a filter connected to the output of the near end of a disturbed channel should not exceed	40.8.6.3	M	Y []	xx mV peak.

40.14.10 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	40.9.1	M	Y []	8-Way connector as per IEC 603-7.
MDI2	Connector used on cabling	40.9.1	M	Y []	plug.
MDI3	Connector used on PHY	40.9.1	M	Y []	jack (as opposed to plug).

40.14.11 General safety and environmental requirements

Item	Feature	Subclause	Status	Support	Value/Comment
ENV1	Conformance to safety specifications	40.11.1	M	Y []	IEC 950.
ENV2	Installation practice	40.11.2.1	M	Y []	sound practice, as defined by applicable local codes.
ENV3	Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection.	40.11.2.2	M	Y []	
ENV4	Care taken during installation to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.	40.11.2.3	M	Y []	
ENV5	Application of voltages specified in 40.11.2.4 does not result in any safety hazard.	40.11.2.4	M	Y []	
ENV6	Conformance with local and national codes for the limitation of electromagnetic interference.	40.11.3.1	M	Y []	
ENV7	All equipment subject to this clause shall conform to	40.11.3.2	M	Y []	the requirements of 14.7 and the applicable sections of ISO11801.

40.14.12 PICS proforma tables for the timing requirements

40.14.12.1 Timing requirements exposed MII :

Item	Feature	Subclause	Status	Support	Value/Comment
TME1	TX-EN (sampled to MDI Output)	40.13.1	M	Y []	7 to 9 bit times
TME2	MDI input to CRS assert	40.13.1	M	Y []	25 bit times
TME3	MDI input to CRS de-assert	40.13.1	M	Y []	29 bit times
TME4	MDI input to COL assert	40.13.1	M	Y []	25 bit times
TME5	MDI input to COL de-assert	40.13.1	M	Y []	29 bit times
TME6	TX_EN sampled to CRS assert	40.13.1	M	Y []	0 to 4 bit times
TME7	TX_EN sampled to CRS de-assert	40.13.1	M	Y []	0 to 16 bit times

40.14.12.2 Timing requirements unexposed MII :

Item	Feature	Subclause	Status	Support	Value/Comment
TMU1	MAC transmit start to MDI output	40.13.1	M	Y []	13 bit times
TMU2	MDI input to MDI output (worst case non-deferred transmit)	40.13.1	M	Y []	50 bit times
TMU3	MDI input to collision detect	40.13.1	M	Y []	33 bit times
TMU4	MDI input to MDI output = Jam (worst case collision response)	40.13.1	M	Y []	50 bit times

40.14.12.3 Timing requirements: carrier assertion/deassertion constraint :

Item	Feature	Subclause	Status	Support	Value/Comment
TMC1	Each DTE shall satisfy the relationship	****	M	Y []	(MAX MDI to MAC Carrier De-assert Detect)-(MIN MDI to MNAC Carrier Assert Detect).

ANNEX 40A Additional Cabling Design Guidelines

The intent of this appendix is to provide additional cabling guidelines when installing a new Category 5 cabling system or using an existing Category 5 cabling system. These guidelines are intended to supplement those in Clause 40. Although the 1 Gb/s specification described in Clause 40 was designed to operate over 4-pair Category 5 cabling systems as specified in ANSA/TIA/EIA-568-A and ISO/IEC 11801, there are additional steps that may be taken by network designers that will provide additional operating margins and ensure the objective BER of 10-10 is achieved.

40A.1 Additional Cabling Specifications

40A.1.1 Multiple-Disturber Power Sum Near-End Crosstalk (PSNEXT) Loss

PSNEXT loss is determined by summing the magnitude of the three individual pair-to-pair differential NEXT loss values over the frequency range 1-100 MHz as follows.

$$\text{PSNEXT\_Loss(f)} = -10\text{Log} \sum_{i=1}^{i=3} 10^{-NL(f)\frac{i}{10}}$$

where: NL(f)i = magnitude of NEXT loss at frequency ‘f’ of pair combination ‘i’,

i = 1, 2 or 3 (pair-to-pair combination).

40A.1.1.1 Multiple-Disturber Power Sum Equal Level Far-End Crosstalk (PSELFEXT)

PSELFEXT loss is determined by summing the magnitude of the three individual pair-to-pair differential ELFEXT loss values over the frequency range 1-100 MHz as follows.

$$\text{PSELFNEXT\_Loss(f)} = -10\text{log} \sum_{i=1}^{i=3} 10^{-NL(f)\frac{i}{10}}$$

where: NL(f)i = magnitude of ELFEXT loss at frequency ‘f’ of pair combination ‘i’,

i = 1, 2 or 3 (pair-to-pair combination).

40A.1.1.2 Alien Crosstalk

40A.1.1.2.1 Multipair Cabling (i.e.; greater than 4-Pair)

Multiple Gigabit Ethernet links ((n*4 -Pair) with n greater than 1) shall not share a common sheath as in a 25-pair binder group in a multipair cable. When the multipair cable is terminated into compliant connecting hardware (TIA does not specify 25 position connecting hardware) the NEXT loss contributions between the adjacent 4-Pair gigabit ethernet link, from connecting hardware and the cable combined, cannot be completely canceled.

40A.1.1.3 Cabling Configurations

The primary application for Clause 40 specification is expected to be between a workstation and the local telecommunications closet, which is generally referred to as the horizontal cabling subsystem in commercial building. As specified in ANSI/TIA/EIA-568-A and ISO/IEC 11801 the maximum length of the cables in the horizontal subsystem is 100 meters, which consists of cords, cables and connecting hardware. The general, or maximum, configuration for the horizontal subsystem is shown in figure 40A-1.

Figure 40A-1—Figure __

On the other hand a minimum configuration can be achieved by removing the jumper cord and transition point, which is shown in figure 40A-2.

Figure 40A-2—Figure __

When installing 1000BASE-T it is recommended that the minimum configuration shown in figure 40A-2 be used. The reasons for using this configurations are:

1. Minimizes the number of interfaces, which minimizes the number of points of component failure.

2. Minimizes crosstalk noise, both near-end and far-end.

3. Minimizes link insertion loss.

4. Minimizes link cost.