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Networks, Routers and Transputers:

Function, Performance and applications

Edited by: M.D. May, P.W. Thompson, and P.H. Welch

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Appendices

Appendix A New link cable connector

A major part of any connection standard is the choice of connector. The connectors mentioned in the section on standards all have major benefits, but no connector combines these benefits. The requirements listed below have been collated from transputer users.

- Ten pins are needed per DS-Link[28]. A connector carrying more than one link should carry two, four, or eight links, with the same pinout and PCB layout for each link;
- The connector should be latched, mechanically sound and robust, but ergonomic so that the end-user finds it easy to plug and unplug;
- The connector should be EMC screened for FCC/VDE/EEC regulations; ideally this should include unused connectors which do not have cables plugged into them;
- It should be able to handle 100 MBit/s signals without introducing serious discontinuities in the transmission line impedance;
- It should be dense enough to allow a reasonable number of separate link connectors, ideally up to ten in the height of a PS2 adaptor or four in the 28mm pitch of an HTRAM;
- Cable connections should be IDC, even from round cable;
- Any mechanical stress should be taken by the mechanical panels and mounting brackets, rather than by the PCB;
- It should be Hard Metric;
- Ideally, versions should be available in the same mechanical dimensions which house a pair of coax or optical fibre connections;
- Reliability is, as always, more important than cost, but the connector should be reasonably low cost and available worldwide.

Several existing connectors come close to meeting these requirements in one or other respect. The latches used in the LEMO cable connectors and SC optical connectors are highly ergonomic and robust. The lanyard latch on some of the LEMO connectors is possibly even better for a high density connector. The modularity, metric dimensions, and high density of the METRAL family from DuPont come close to meeting some of the requirements. There are a number of good cable connectors to fit backplanes, one of the closest to the requirements being the Fujitsu FCN-9505/9506 which combines modularity, robustness and good screening.

The new connector pulls together the best features of these connectors.

This 10-way modular I/O connector system has been designed by AMP, Fujitsu, and Harting, in cooperation with INMOS/SGS-THOMSON. Pins are on 2mm pitch to give a height small enough to fit the mounting brackets of personal computer cards, and connector pitch is 6mm.

The resulting connector: is Hard Metric, in line with IEC 917; is screened, to aid compliance with EMC regulations; has a leading 0V pin for reliable ‘hot-swap’; has eight pins for buffered differential DS-Links, together with a pin for remote power; is exceptionally dense, with two to five times as many connectors in a given panel length compared with existing connectors; and fits all the board standards such as PC, VME, SBus as well as those based on IEC 917. A particular benefit of the connector is that it allows equipments to benefit from a large number of ports, in the

28. Two differentially–buffered data/strobe pairs (8 pins), one leading ground pin, and power for remote devices.

same way as DS-Links make it possible to build a routing-switch-chip with a large number of ports.

INMOS have built the connector into prototype PCBs for the T9000, and presented the work on the connector (together with other aspects of proposed standards for DS-Links) to ESPRIT partners and to several IEEE and ANSI standards working groups.

There is now full agreement between the connector manufacturers and INMOS on all aspects of intermatability of the connector, with minor changes having been agreed as a result of building and using the prototypes. The connector's electrical and mechanical robustness, its density, modularity and ergonomics, are widely applicable to electronics which becomes ever smaller.

Without the new connector, standards are still possible. For example office equipment such as terminals, laser printers, disks, and fax machines, each of which might use from two to four of the connectors, could use one type of connector; and computers, which might use many more connectors, use a different type. But there are obvious advantages in using the same connector for all the equipments. In some respects, the links would become a 100 MBit/s RS232, with autobaud and a simple packet routing protocol built in.

The new connector is not limited, however, to use with transputer links. There are many other interfaces which use point-to-point connections, and there is a huge number of 9-way D connectors installed around the world. As electronic equipment gets smaller, connectors begin to dominate the size of the equipment. Much work has gone into increasing the density of the connectors, but usually with a view to having more ways in the same space. This proposal uses these improvements in density to fit the same small number of ways into a smaller space.

Although the new connector has been derived from the needs for transputer links, it appears therefore that such a connector would meet the generic needs of the computer and electronics industries.

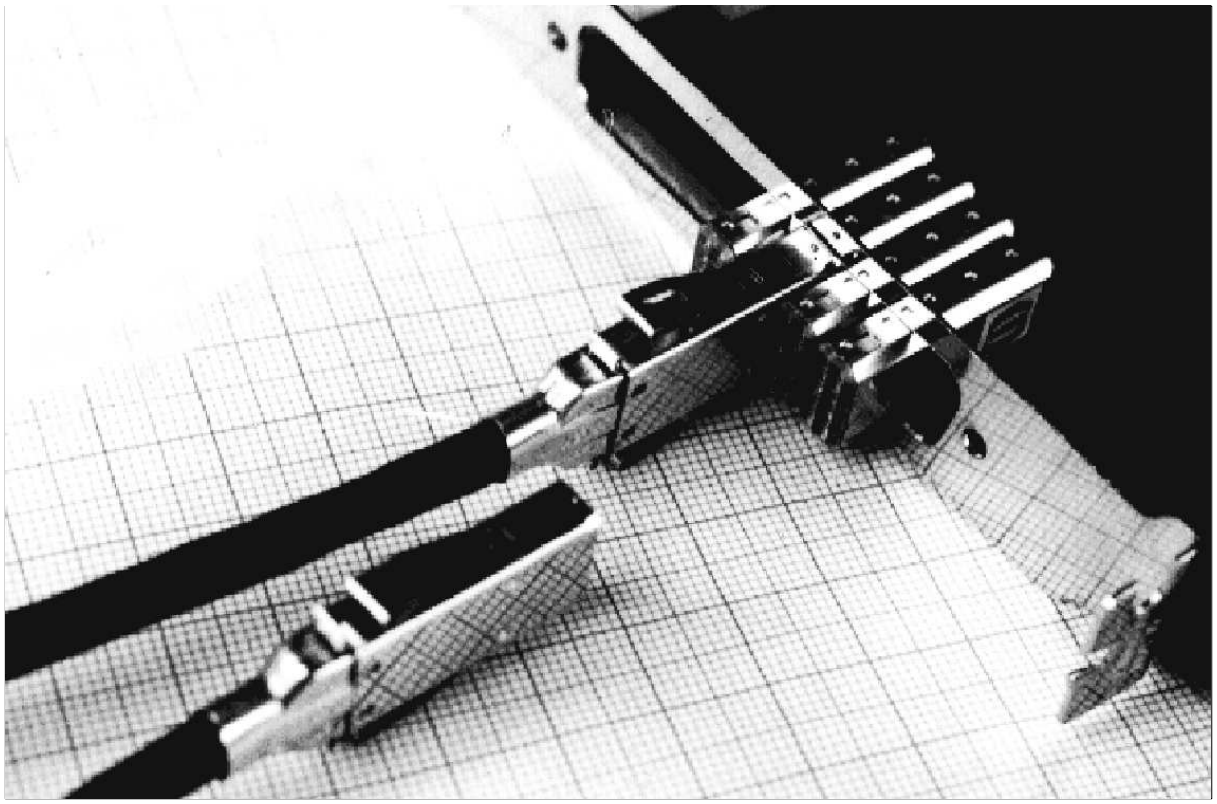

Figure A.1 Prototypes of the link new connector

Appendix B Link waveforms

A few example oscilloscope traces are shown of the waveforms seen with different lengths of connection and with different forms of buffering. The waveforms on this page are from simulated link signals: figure B.1 shows isolated 5ns pulses, with less than 1.5ns distortion resulting from the driver, receiver, and 10m of 30 AWG cable; figure B.2 shows waveforms from simulated link signals before and after transmission through 41 series buffers, the circuitry described in HP's Application Bulletin 78, and 100m of fibre (waveforms are identical when using Honeywell optical components).

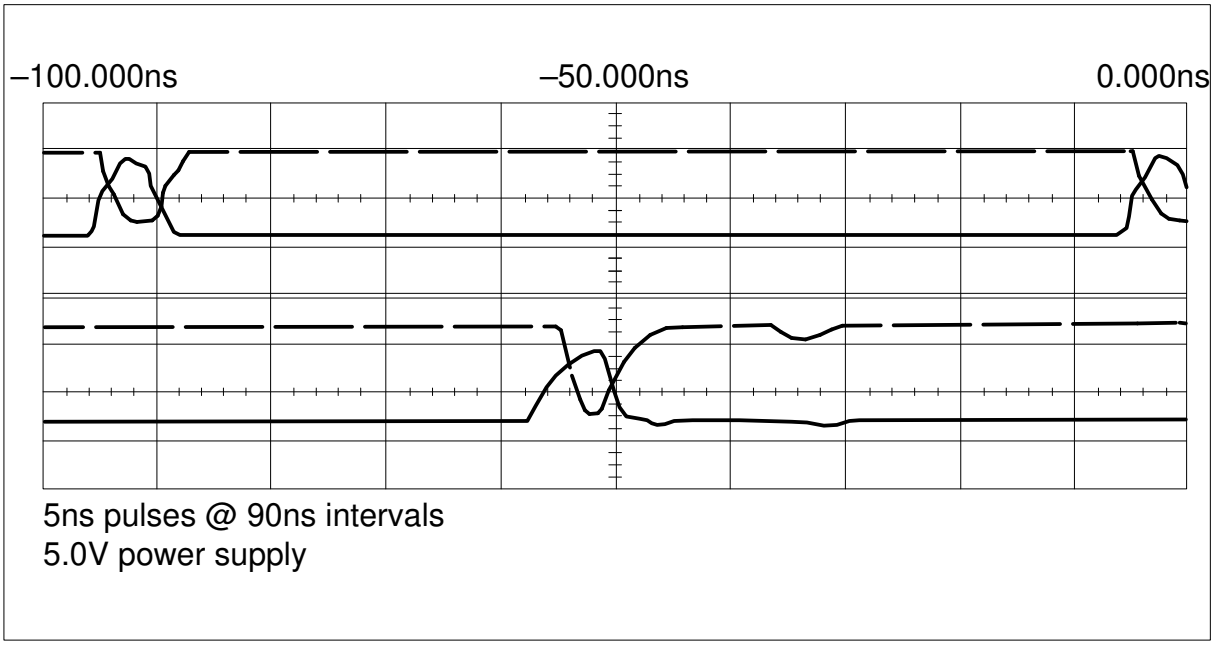

Figure B.1 Isolated 5ns pulses, AT&T 41M series, 10m × 30AWG

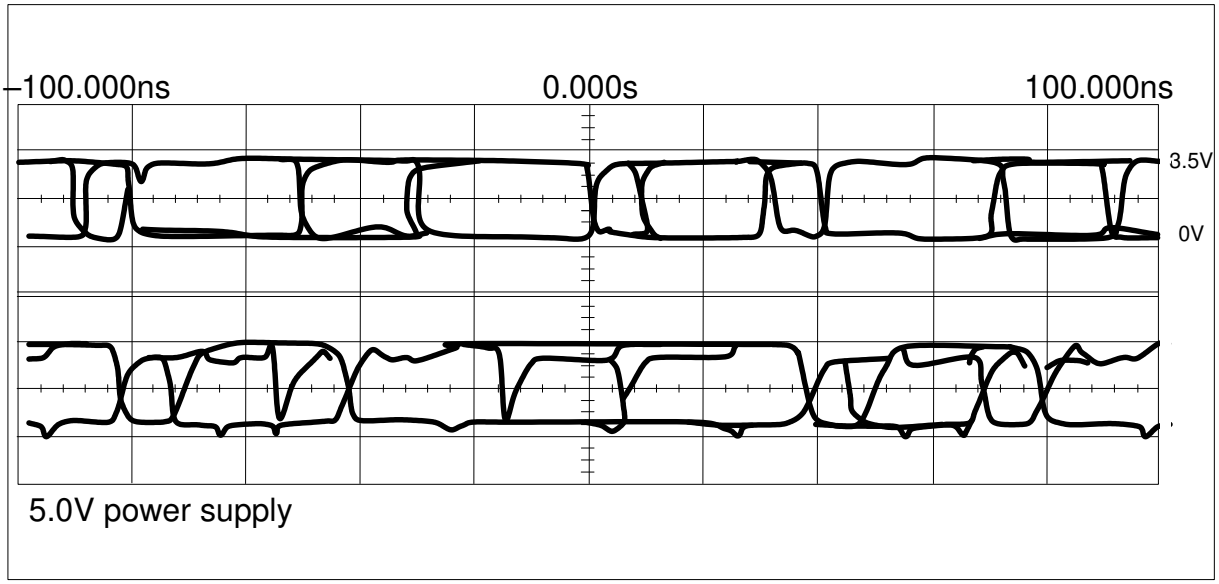

Figure B.2 HP1414 LED, 2416 receiver, 100m of 62.5µ fibre

The figures B.3 and B.4 on this page show actual link waveforms, which were correctly received through the 41 series driver and receiver and 30m of cable. Note the attenuation of the differential pseudo ECL signal apparent in figure B.3.

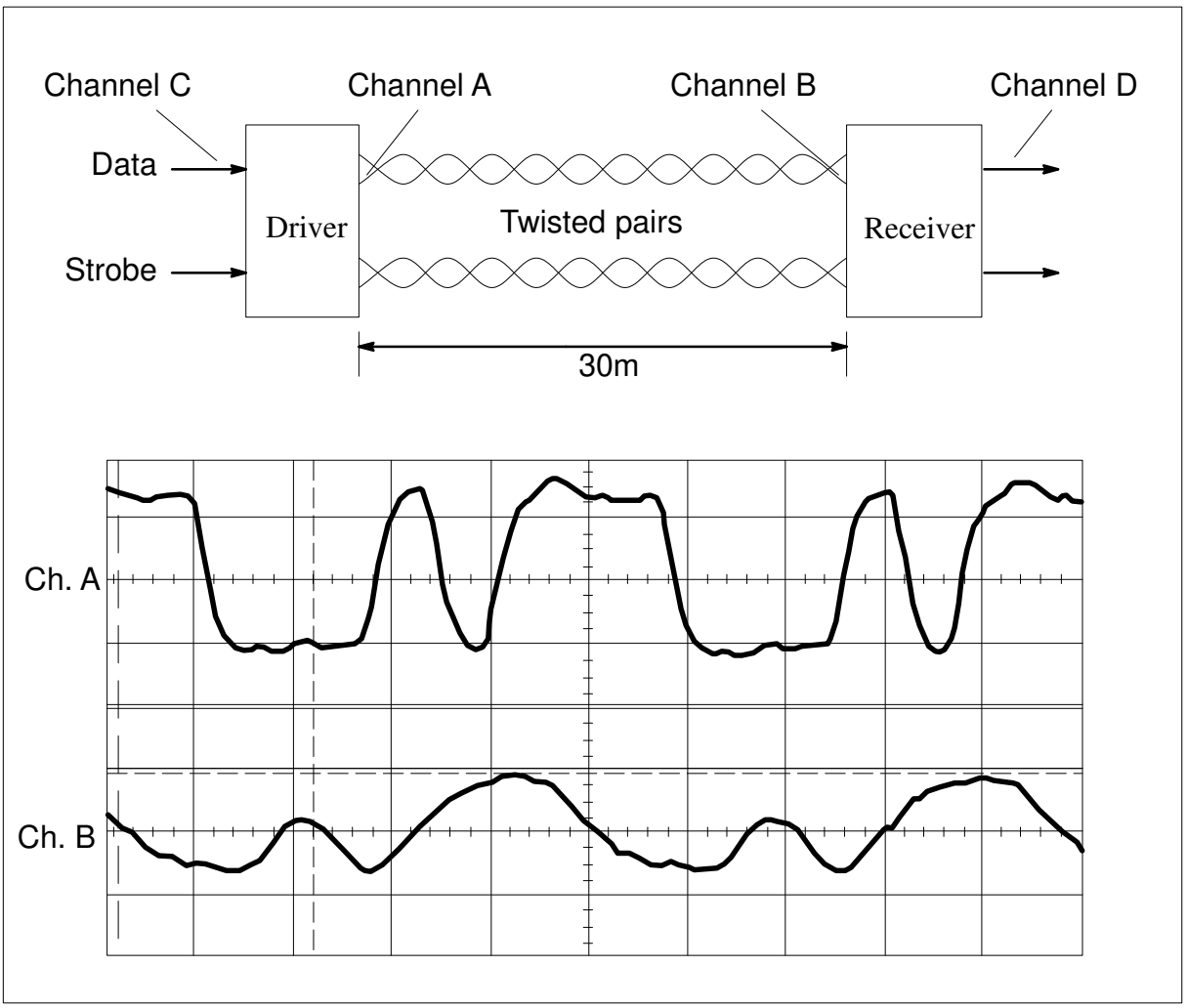

Figure B.3 DS-Link idle pattern, AT&T 41 series buffers

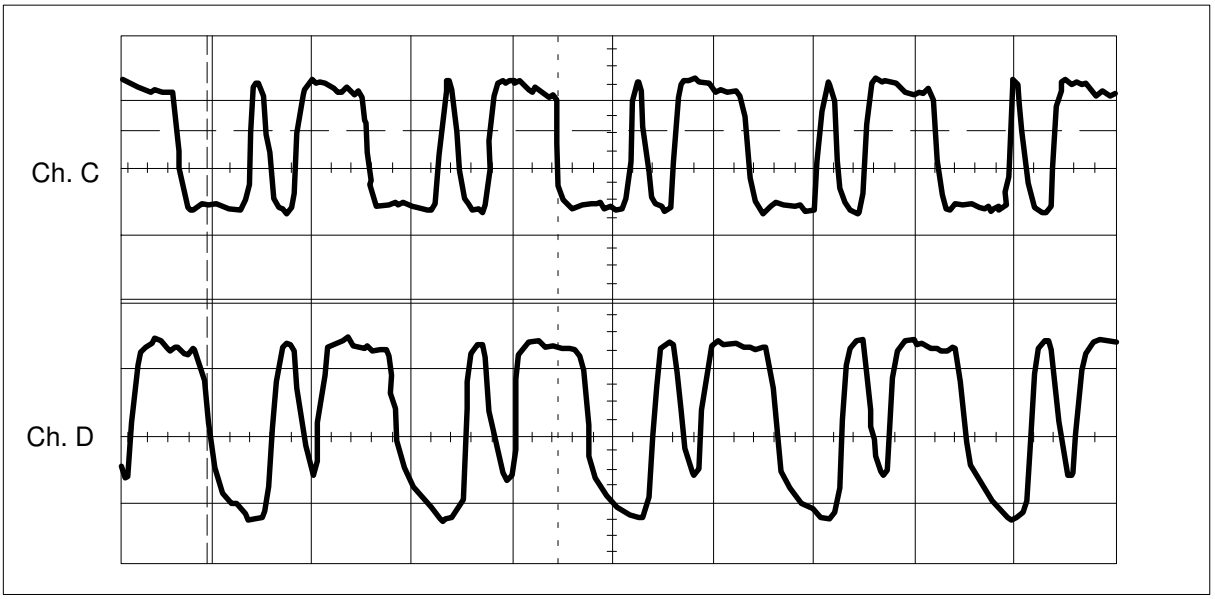

Figure B.4 TTL signals corresponding to figure B.3

Appendix C DS–Link Electrical specification

The DS–Link is designed for point to point communication which may be on a single pcb, board to board or box to box. Since this implies that transmission line problems will be present, the electrical level has been designed as a transmission line system. In order to reduce the power required for each link (enabling the use of many links) source only termination is used. The choice of impedance level (nom. 100 Ω)was made such that it is straight–forward to make these transmission lines with standard pcb materials.

The DS–Link connection at the electrical level usually comprises three parts: Link output driver, transmission line and link input pad (see figure 1). These parts are duplicated to provide the Data and Strobe wires for the DS–Link. The return connection is made from a similar pair of connections, thus there are four wires in all, two in each direction. The output driver has a controlled output impedance to reduce reflection problems. The transmission line is provided by pcb, coax or other suitable controlled impedance interconnect. The input pad is designed as a standard TTL input and has no internal termination.

Link Output pad

Since this system is effectively a driver driving an open circuit transmission line, careful consideration must be made to damp reflections from the load. This is catered for by providing an output driver which is designed such that reflections from it do not adversely affect the voltage received at the receiving end of the transmission line. To achieve this the driver has a controlled output impedance even when switching. Due to processing variations an exactly terminated line is not possible and nominal termination values other than 100 ohms have been used to ensure the receiving input does not receive spurious data or glitches. Since TTL thresholds are not balanced with respect to the power supplies, the pulling high output impedance is in fact different from the pulling low output impedance.

Output driver parameters

The following list of parameters covers the full range of processing, temperature and supply voltage encountered by a DS Link. Vdd may have the range 4.5 to 5.5V , Tj (junction temperature) in the range 0 to 100 degrees C. **Note that they apply to the implementation of the DS–Link current when this book went to press; for information relating to a specific product, the appropriate datasheet should be consulted**.

Parameter	Min	Max	units	Notes
fmax maximum operating data rate (as part of a DS–Link)	100		Mbits/s	**1**
tr output rise time	2.5	6	ns	**1,2,4,6**
tf output fall time	2.5	6	ns	**1,2,4,6**
tph output high time for a nominal 20ns bit period (1.5v threshold)	15.8	24.2	ns	**1,2,4,5,6**
tpl output low time for a nominal 20ns bit period (1.5v threshold)	15.8	24.2	ns	**1,2,4,5,6**
Voh Io= 1ma	Vdd–0.4	Vdd	Volts	**3**
Vol Io=–1ma	0	0.4	Volts	**3**
Rl Output impedance, output driving low Vo=1volt	63	104	Ohms	**3**
Rh Output impedance, output driving high Vo=Vdd–1volt	110	247	Ohms	**3**

Note 1. Using the test circuit shown in figure C.1
Note 2. Measured at point **B** on the test circuit (figure C.1)
Note 3. Measured directly (without test circuit)
Note 4. Sample tested and/or characterised only
Note 5. Allowance made for a ground difference of up to 0.4 Volt between transmitting and receiving devices.
Note 6. See figure C.2

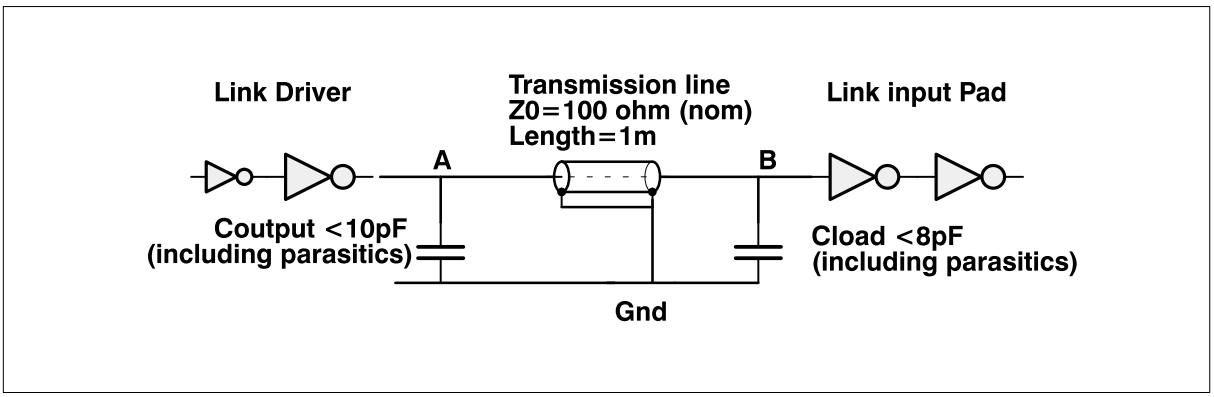

Figure C.1 Test Circuit

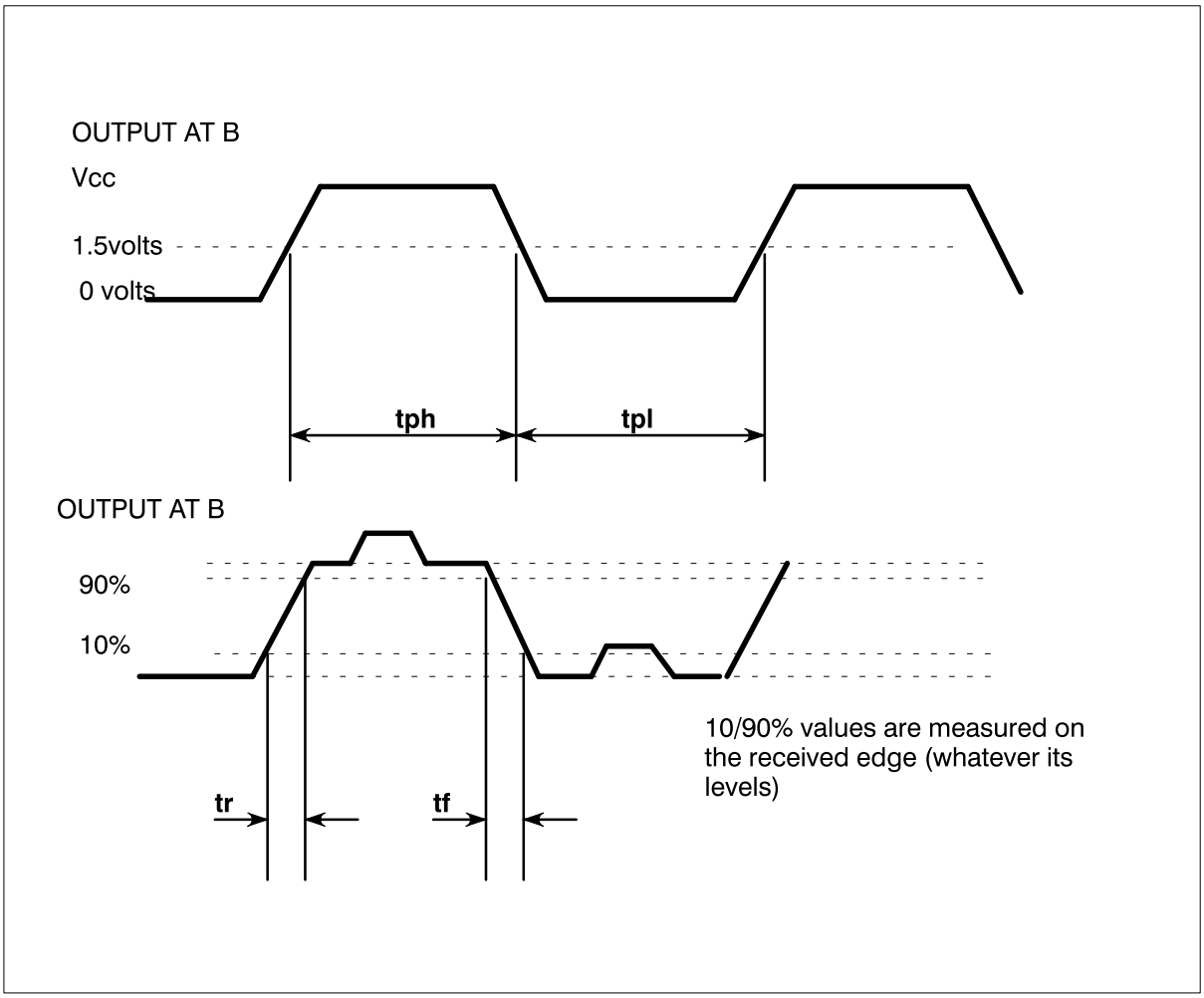

Figure C.2 DS–Link Timing

Transmission line requirements

Careful consideration must be made when connecting link output drivers to their corresponding receivers. For distances of greater than 20cm the link line must be considered as a transmission line. Discontinuities or variations in characteristics impedance should be kept to a minimum. The transmission line may be made on pcbs but care must be taken to provide a good ground or power plane beneath the link track and crosstalk should be minimised with other tracks (including between data and strobe lines of the same link). This can be helped by placing grounded tracks either side of the link track, as described earlier. The longest length of line achievable will depend on the materials used for interconnect and the grounding arrangements. **Note that they apply to the implementation of the DS–Link current when this book went to press; for information relating to a specific product, the appropriate datasheet should be consulted.**

Recommendation	Min	Max	units
Zo Characteristic impedance	90	110	ohms
tskew difference in transmission line propagation delay between data and strobe lines for DS–Link operating at 100 MBit/s	–4	4	ns

Link Input Pad

The link input pad is a standard TTL compatible CMOS input pad. Care should be taken not to introduce too much capacitance on the link line near the receiving input buffer. **Note that they apply to the implementation of the DS–Link current when this book went to press; for information relating to a specific product, the appropriate datasheet should be consulted.**

Parameter	Min	Max	units	Notes
fmax maximum operating data rate (as part of a DS–Link)	100		Mbits/s	
Vih Input high voltage	2.0	Vdd+0.5	Volts	
Vil Input low voltage	–2	0.8	Volts	**1**
Iih input leakage current, Vin=2.0volts	–10	10	uA	
Iil input leakage current, Vin= 0 to Vdd volts	–10	10	uA	
Cin Input capacitance measured at 1MHz		7	pF	**2**

Note 1. Input voltages of less than –0.5 volts should only be transient in nature.
Note 2. Sample tested

Appendix D An Equivalent circuit for DS–Link Output Pads

The following preliminary equivalent circuit may be used to simulate the output from DS–Link pad drivers found on the IMS T9000, C100, and C104 devices. It has been done in such a manner that any circuit simulator (provided it can model inductors) will be capable of modelling the link pad driver, with no reliance on any specific device models.

The circuit (figure D.1) should be constructed from idealised components with the parameters listed below. For simulation time reasons it may be preferable to add a small capacitance (e.g. 100f) between the MOS device drains and their respective supply. In addition it is more realistic to add a supply–to–supply capacitance for the IC which will depend on which chip the DS–Link is on. This can be 1uF for a T9000 to only a few 100pF for a C100. The waveforms (figure D.2) can be straight line representations (e.g. SPICE Piecewise Linear) , bearing in mind 10/90% times are quoted.

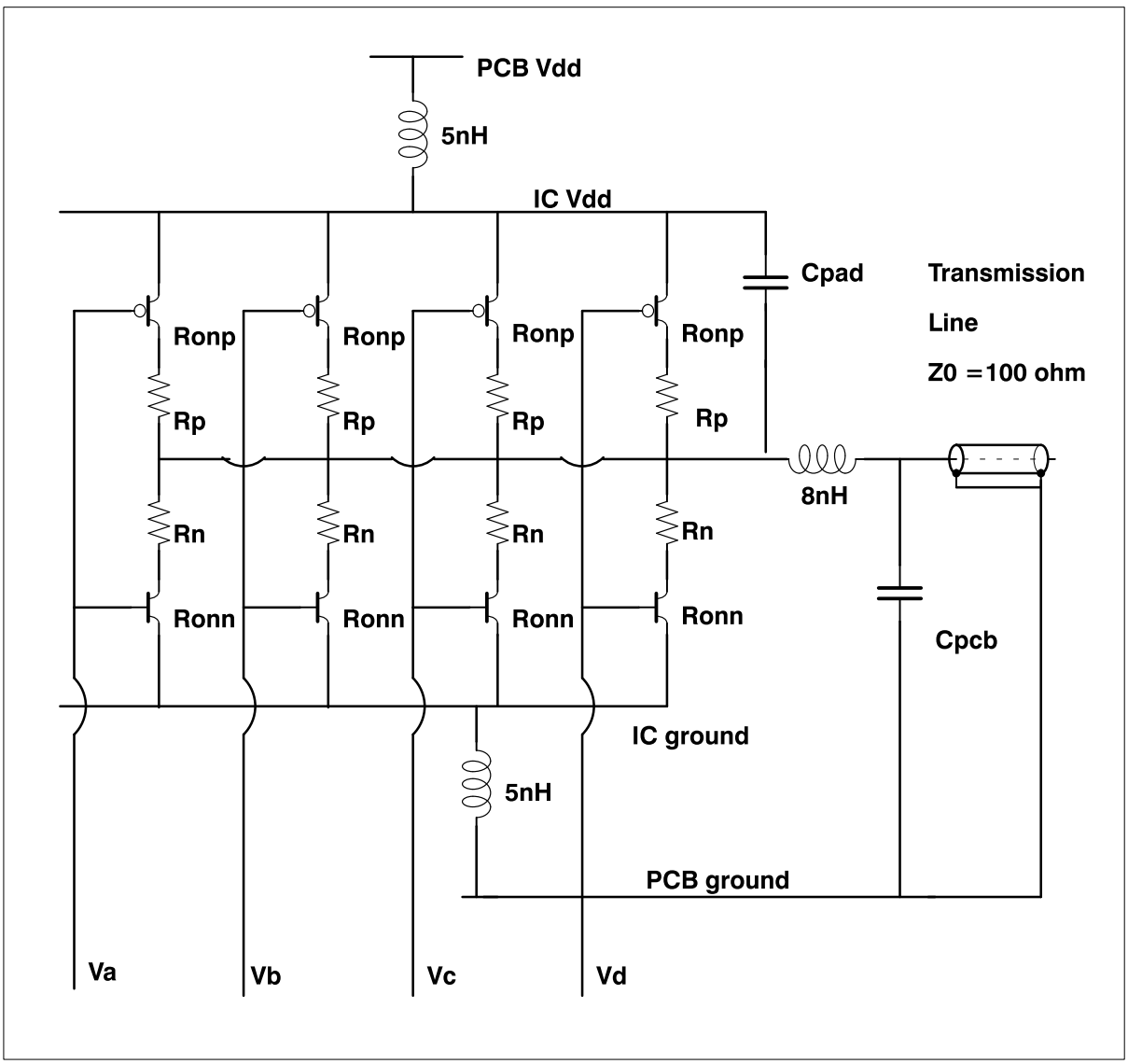

Figure D.1 Equivalent Circuit

Key parameters

The following list of parameters covers the full range of processing, temperature and supply voltage encountered by a DS–Link. Vdd may have the range 4.5 to 5.5V. **Note that they apply to the implementation of the DS–Link current when this book went to press; for information relating to a specific product, the appropriate datasheet should be consulted**.

Parameter	Min	Max	units
Ronp, Vds=–1Volt	106	481	Ohms
Ronn, Vds=1Volt	25	82	Ohms
Rp	332	508	Ohms
Rn	227	333	Ohms
tpd, rising and falling transitions	0.66	2.0	ns
tf, 10/90% of Vdd Va,Vb,Vc,Vd	1.2	2.3	ns
tr, 10/90% of Vdd, Va,Vb,Vc,Vd	1.5	2.8	ns
Cpad	0.5	0.5	pF
Cpcb, any interconnect before transmission line.	2.0	As board layout dictates	pF

In SPICE simulations the following model may be used for the transistors:

.model n nmos Level=1 vt0=0.7 kp=50u tox=40n
.model p pmos Level=1 vt0=0.7 kp=20u tox=40n

This leads to the following transistor sizes (at 27°C only):

Ronn(max) w=55u,l=1u
Ronn(min) w=175u, l=1u
Ronp(max) w=23u, l=1u
Ronp(min) w=102u, l=1u

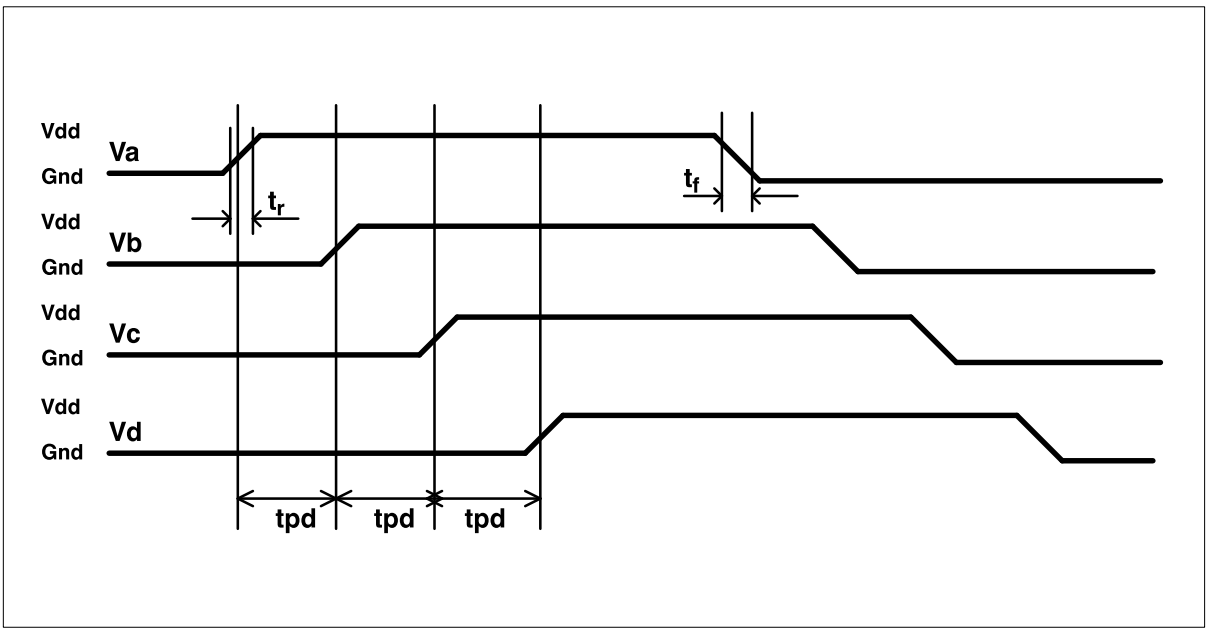

Figure D.2 Output Pad Timing