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Function, Performance and applications

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This chapter was written by C. Barnaby and N. Richards.

- One ATM cell in 2 T9000 packets:–
    - One 32–byte data packet
    - One 21–byte data packet

Both unidirectional and bidirectional use of the DS-Links is considered in the following analysis. Data rates and throughput are calculated for DS–Links operating at 100 and 200 Mbits/s to give a representative performance spread.

10.4.2 Unidirectional Link Use

Single 53–byte packet

Suppose that the 53–byte ATM cell is sent as a single 53–byte packet. The packet has a one byte packet header and a four bit packet terminator. The flow control overhead is rounded up to one flow–control token, of four bits, per ATM cell. The total number of bits transmitted is the sum of the data bits, the header bits, the terminator bits, and the flow control bits, with the DS–Link transferring a byte of information as 10 bits.

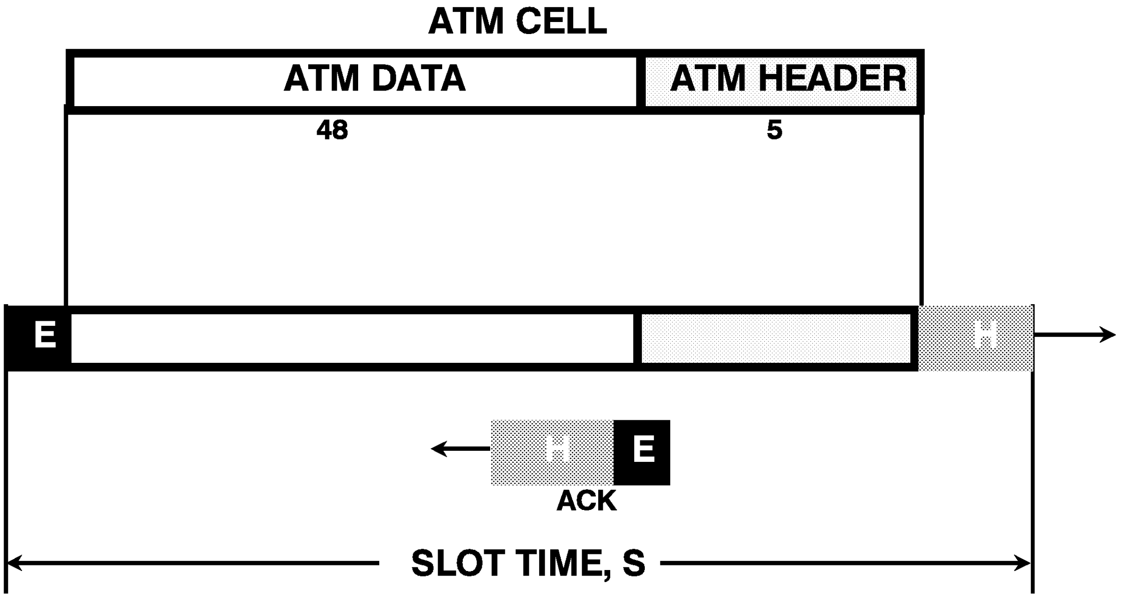

Figure 10.28 Unidirectional Single–Packet ATM–DS-Link Mapping

The net bandwidth available for the ATM traffic in this configuration has been calculated and is presented in Table 10.1 at the end of this section.

Double Packets

Now suppose that the largest packet contains 32 bytes of data, as is the case for a T9000. The 53–byte ATM cell will be transmitted as 2 packets, one 32 bytes long, the other 21 bytes. Each packet has a one–byte header and a 4 bit terminator. Again the overhead of flow control tokens is less than one token per ATM cell, and is rounded up to one token per ATM cell. This is an extra 4 bits.

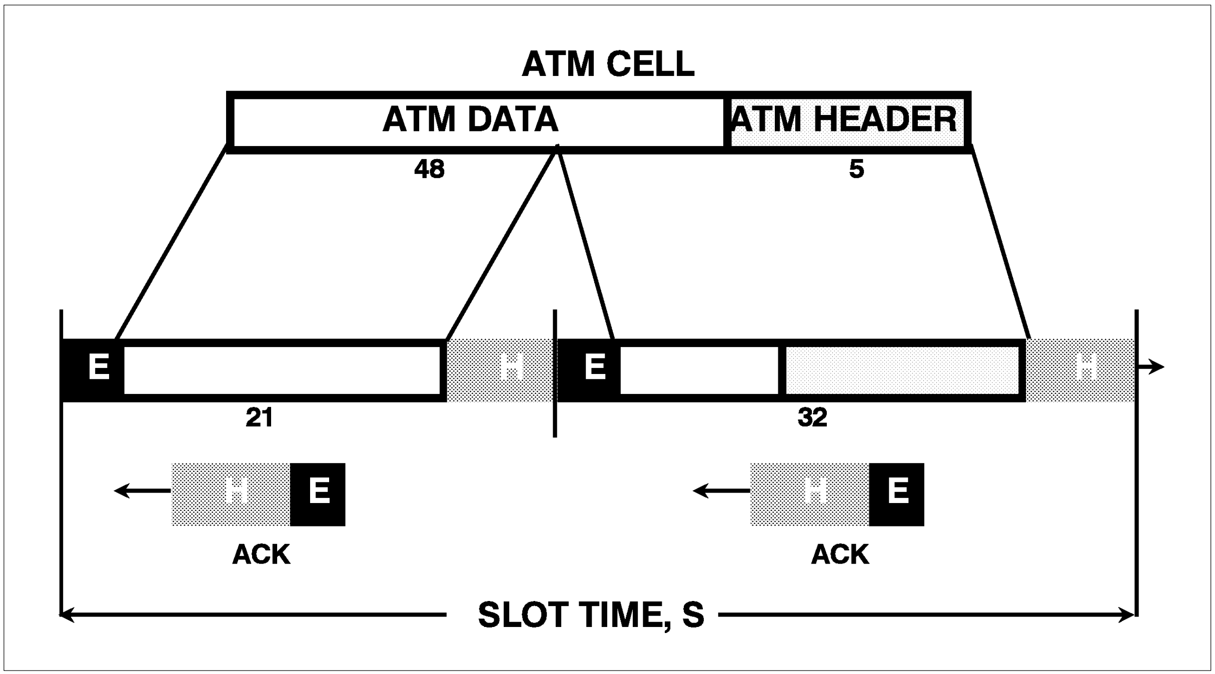
ATM CELL
ATM DATA
ATM HEADER
48
5
E
H
E
H
21
32
H
E
ACK
H
E
ACK
SLOT TIME, S

Figure 10.29 Unidirectional Double–packet ATM–DS-Link Mapping

Again, the bandwidth results are presented in Table 10.1 at the end of this section.

10.4.3 Bidirectional Link Use

When considering the effect of bidirectional operation, it is assumed that the inbound link carries a similar traffic load to the outbound link.

For bidirectional link use, the link overheads are greater. The link carrying the outbound data must now carry the acknowledge packets for the data on the inbound link, and vice versa. An acknowledge packet consists of a one–byte packet header, and a four–bit packet terminator. The outbound link must also carry flow control information for the inbound link.

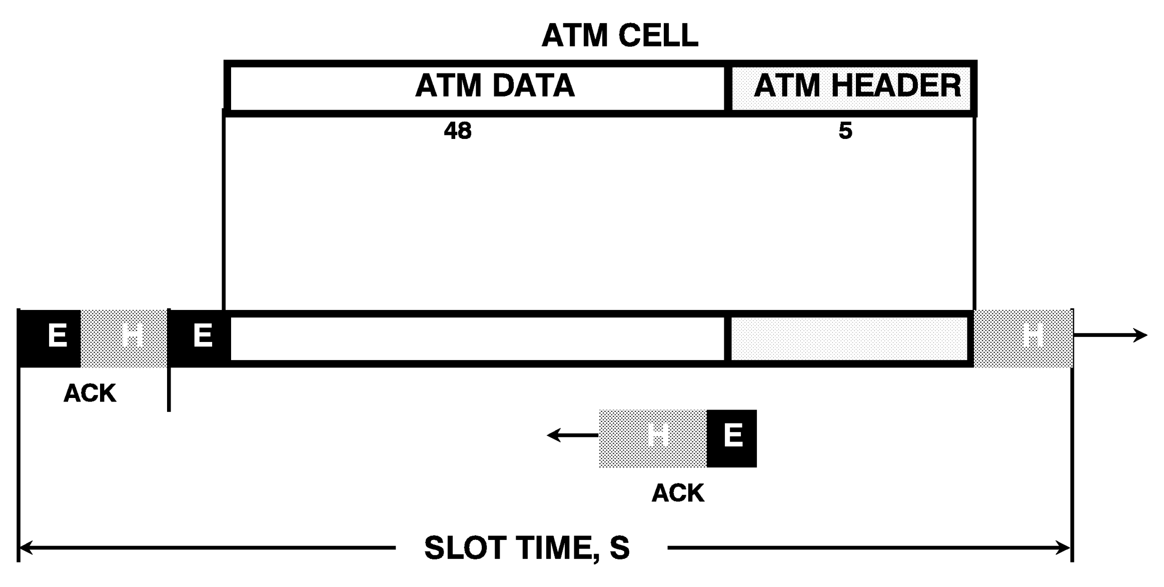
ATM CELL
ATM DATA
ATM HEADER
48
5
E
H
ACK
E
H
H
E
ACK
SLOT TIME, S

Figure 10.30 Bidirectional Single–Packet ATM–DS-Link Mapping

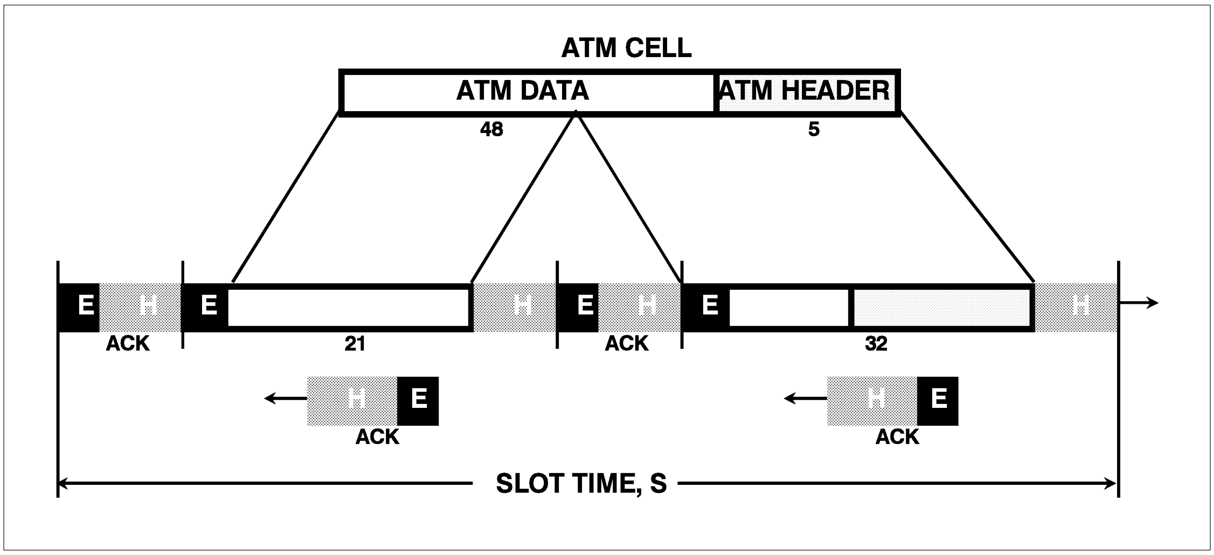

Figure 10.31 Bidirectional Double–Packet ATM–DS-Link Mappings

The results are presented in Table 10.1.

10.4.4 Summary of DS–Link Results

The performance results of the above configurations are summarized in the following table. The bidirectional throughput is available simultaneously in both directions on the link.

Link Speed (Mbits/s)	Max Packet Size (bytes)	ATM Cell Throughput (Mbits/s)		ATM Cell Rate (Cells/s)	
		Unidirectional	Bidirectional	Unidirectional	Bidirectional
100	32	75	69	177k	163k
	53	77	72	182k	175k
200	32	150	138	354k	325k
	53	154	144	363k	340k

Table 10.1 ATM Performance over DS-Links

The results indicate that 100 Mbits/s links would be more than sufficient to carry ATM at T3 rates, say sub–50 Mbits/s, so could be used to provide an economical point–to–point local connection from a terminal into an ATM concentrator. The DS-Link speed can be varied anywhere from 10 Mbits/s upwards in 5 Mbit/s increments, so the bit rate could be set appropriate to the physical medium used (only the transmit speed needs to be set, the receiver is asynchronous).

At 200 Mbits/s the DS-Links could provide a full–rate ATM connection unidirectionally and an only marginally slower (144 Mbit/s) bidirectional one, although if the traffic flow was asymmetrical this rate could be improved.

For interconnect use within a C104 switching fabric, single 200 Mbits/s DS-Links could provide full performance. However, traffic congestion issues would be far more significant than the marginal DS-Link bandwidth, so the use of grouped link pairs would be beneficial for blocking/congestion reasons. Assuming the fabric could support at best only 80% per–link throughput (based on the simulation models for a hypercube with Universal routing), this would mean that any DS-Link pair running at a bit–rate from about 120 Mbits/s up would support full–rate ATM traffic through the switch fabric (for a more complete treatise, see Chapter 7).

10.5 Conclusions

In this paper the use of the transputer architecture, its multiprocessing capability, its communication links and its packet switching interconnect capability, has been described in terms of applications within the emerging ATM systems market. Applications within public switching, private switching/internetworking and terminal adaption equipment have been considered. The main motivation in these discussions has been the convergence of architectures necessary to support message–passing multiprocessing computers (such as the transputer) and fast–packet switching systems (such as ATM). As each technology evolves and matures it is reasonable to expect an even closer relationship between the two.

A distinction has been drawn between the use of the transputer architecture in public versus private switching systems. In high–speed public switches the T9/C104 architecture is offered as a multiprocessing architecture for the *control plane* of the switch, with ATM traffic carried by a separate, dedicated (usually proprietary) switching fabric. Lower–speed private customer premises equipment has the potential to use a C104–based switching fabric directly, which could be used to carry both control **and** data traffic.

The use of transputers as uniprocessors, as opposed to multiprocessors, for building network termination and terminal adapter cards has also been considered. This area has a different set of constraints, mainly driven by cost, since ATM adapters and line cards will represent the volume end of the market. Silicon integration is the key, and the move to semi–custom techniques for transputer technology is an important factor here.

Given economical drivers for fibre and twisted pair, the DS-Links themselves offer their potential as a low–cost physical interconnect between terminals (PC's and workstations) and a local C104–based ATM concentrator. Transporting ATM cells and protocols across a DS-Link physical medium is very straightforward and provides relatively cheap office–scale connections with the added advantage of a built–in flow–control mechanism back to the source.

ATM is an exciting field and the transputer architecture offers a multitude of possibilities for building ATM systems. There are numerous combinations of ideas possible and no doubt in time many unique and interesting variations will emerge.

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