

M50530-XXXFP

24. Feb 1991

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

DESCRIPTION

The M50530-XXXFP is an LSI for a dot matrix liquid crystal display control drive which has been developed by making use of the silicon gate CMOS process, and can control multi-digit data and directly drive a dot matrix liquid crystal display of 256 font types including alphanumerics, kana characters and symbols by a simple control from μ c and μ p.

The M50530-XXXFP offers a system for controlling and driving a dot matrix liquid crystal display, and also expands the number of display digits by the simultaneous use of the IC for the liquid crystal drive, M50521FP or M50524FP.

By using the M50530-XXXFP it has been possible to create a liquid crystal display system which is compact, has low power consumption and is very versatile.

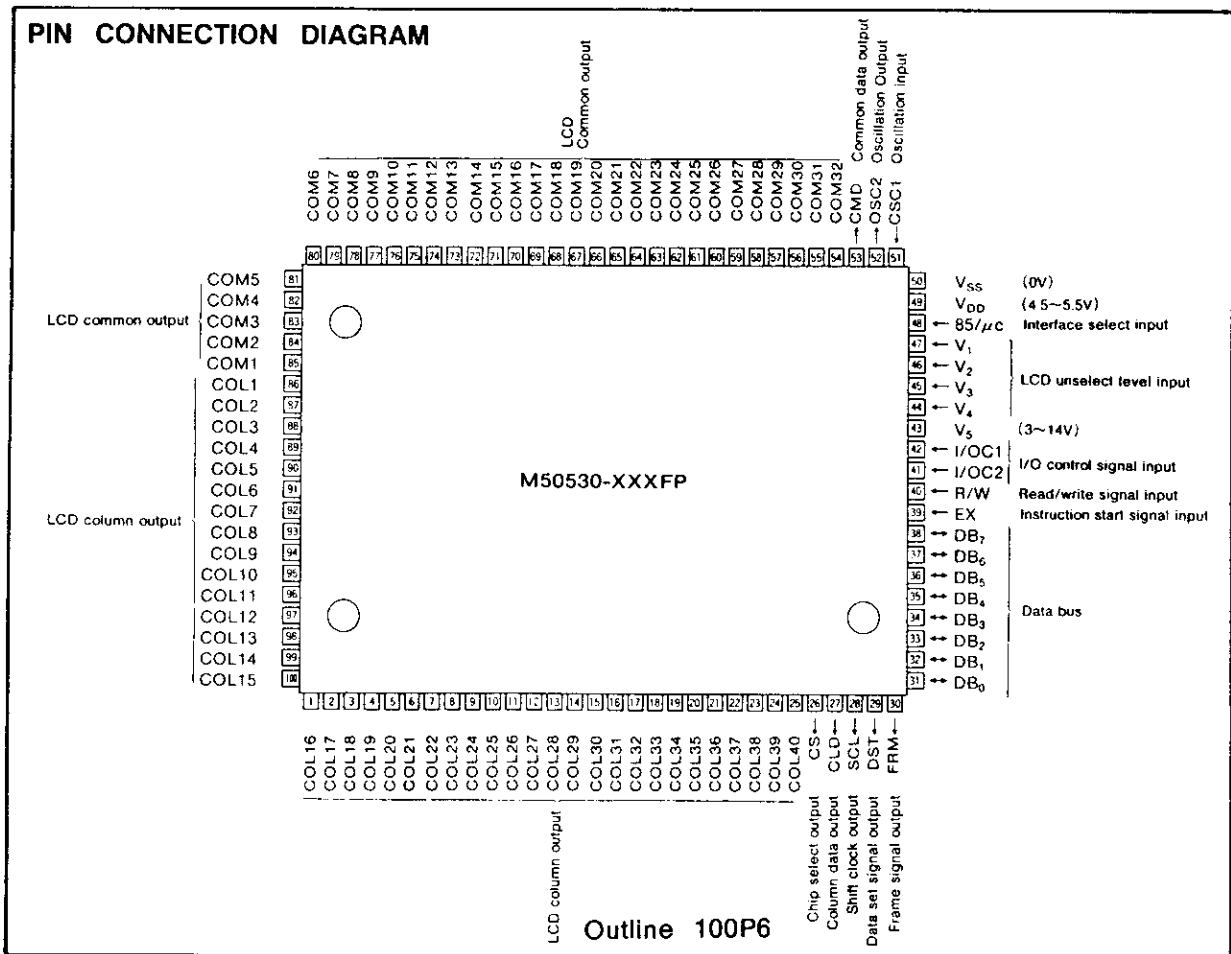
FEATURES

- Interfacing (It is possible to interface directly with a 4-bit μ c and an 8-bit μ c. It is possible to interface directly with 8085 μ p.)
- Characters (256 font types with 5X8 dots or 5X12 dots [cursor is common to both])
- Memory (Generally for a display data RAM and for a character generation RAM, it is possible to use

a total of 256 words, with 9 bits to a word, and to select one configuration out of the 4 types described below that offer maximum and minimum configurations.)

- Display Data RAM (hereafter referred to as DD RAM)
9 bits to a word (of these, 1 bit is used to underline)
..... 4 types from a maximum of 256 words to a minimum of 160 words
- Character generator RAM (hereafter referred to as CG RAM)
5X7 dots..... 4 types from a minimum of 0 to a maximum of 12 characters
or 5X11 dots..... 4 types from a minimum of 0 to a maximum of 6 characters
- Character generator ROM (hereafter referred to as CG ROM)
5X7 dots..... 4 types from a maximum of 256 to a minimum of 244 characters
or 5X11 dots..... 4 types from a maximum of 256 to a minimum of 250 characters

PIN CONNECTION DIAGRAM

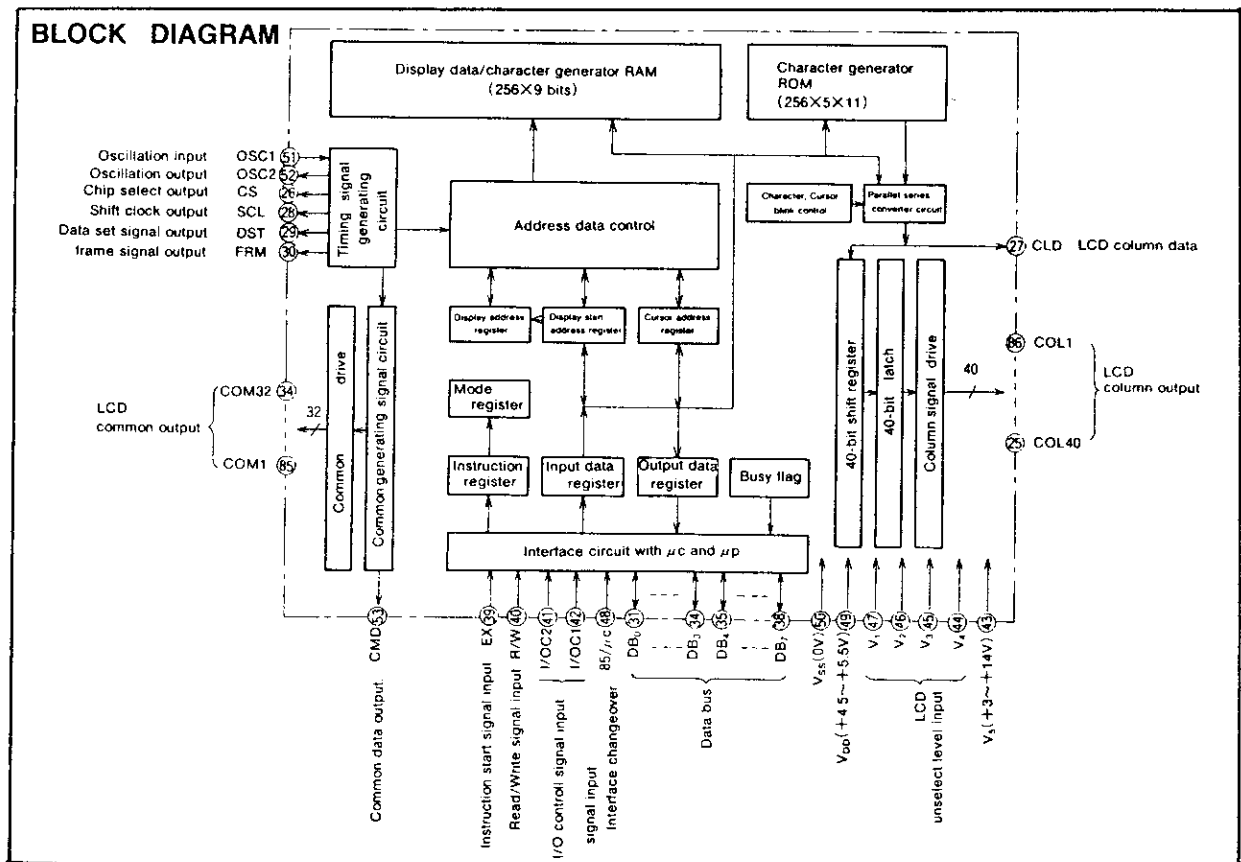


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- Instructions (The following comprehensive instructions are given.)
 - Cursor address set-up for DD/CG RAM
 - Display start address set-up
 - Data write and read from RAM
 - Display shift and cursor shift
 - Interface changeover between 8-bit μ C/4-bit μ C
 - Font changeover between 5 $\times$ 8 dots /5 $\times$ 12 dots
 - Duty changeover between (1/8, 1/12), (1/16, 1/24), and (1/32, 1/48)
 - Selection between DD/CG RAM configurations
 - Underline set-up for each character
 - Display ON/OFF, cursor display ON/OFF, underline display ON/OFF, character blink, and cursor blink
 - Blink frequency set-up
 - Display address home and cursor address home
 - Clearing entire display
- Display digit No. :
 - 1 chip system (8 digits for 1 line, 8 digits for 2 lines, and 8 digits for 4 lines)
 - Maximum system configuration (The 4 following types of maximum system configuration are available for 1 line, 2 line, and 4 lines respectively.)
 - 1 line 256 digits, 244 digits, 192 digits, and 160 digits
 - 2 lines 128 digits, 112 digits, 96 digits, and 80 digits
 - 4 lines 64 digits, 56 digits, 48 digits, and 40 digits
- Internally provided for liquid crystal display drive circuit
 - Common signal: 32 lines (corresponds to 4-line portion for 1/32 duty)
 - Column signal : 40 lines (corresponds to 8-digit portion for 5 lines per digit)
 - By using the IC for the liquid crystal drive M50521FP or M50524FP, it is possible to expand the display to the maximum number of digits.
- Automatic reset at power cut-off
- Built-in oscillator (An external resistor or an external ceramic filter)
- Oscillation frequency 2.58MHz (for a frame frequency of about 70Hz)
- Column data transfer speed (1.29Mbit/set [for oscillation frequency of 2.58MHz])
- Blink frequency (About 0.5Hz, 1Hz, 2Hz, and 4Hz [for oscillation frequency of 2.58 MHz])
- Supply voltage for logic circuit : (+4.5~5.5 V)
- Output voltage of liquid crystal drive : (+3~14 V)
- On-resistance of liquid crystal drive :
 - 500 Ω (14V) and 2k Ω (5 V), maximum
- Low power consumption : Silicon gate CMOS process
- Package : 100-pin plastic flat QUIP, lead pitch 0.65mm

APPLICATION

OA apparatus (portable personal computer, electrical typewriter e.t.c), Information apparatus (Telephone, Fax e.t.c).



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FUNCTIONAL DESCRIPTION

The LSI M50530-XXXFP is controlled by instructions from a μc or μp on the outside. In other words, the μc or μp takes the role of master processor and M50530-XXXFP takes the role of slave processor. M50530-XXXFP can control completely the liquid crystal display (LCD).

When transferring data between the μc or μp and the internal RAM within the M50530-XXXFP first the RAM address is set by an instruction in the cursor address register, then, either external data is written by an instruction in the internal RAM via the internal input data register or data is read by an instruction from the RAM to the outside via the output data register.

M50530-XXXFP has various execution condition modes for instructions such as function construction, display, reading, writing etc. In this way, the efficiency of execution of the instruction has been improved. These different modes are stored by the mode setting instructions in the mode register, and they are used in subsequent instructions as execution conditions.

When RAM data is displayed by LCD, the address of the RAM data to be displayed as the first digit on the left-hand side of the LCD is set with the display start address. First, set by instruction the first digit in the display start address register to the RAM address desired for display. Data is displayed by LCD from this address to successively higher digits.

As regards the LCD drive, a common signal is generated in the timing generation circuit on the scanning side to drive the common side of the LCD via the common signal drive.

The RAM data for display, designated by the address in the display address register is read on the column data side as a character code. The data is then converted to a character pattern in the character generator of the ROM or RAM.

Then, by sending the 5-bit data in the line, which corresponds to the common scanning signal in the line matrix of the character pattern, to the shift register as a column signal, the column side of the LCD is driven via the column signal drive.

In order to display all of the display data by LCD: 1) the display address register is incremented for each of the common signals; 2) display data is read successively from the RAM; 3) column signals for all lines of the display are sent, by repeated conversion and transfer, to the column drive; and 4) the column side is driven.

The LCD operation is independent of the execution of an instruction from the outside and is processed within a prescribed time, so that no flickering will be generated in the display regardless of the presence of instructions being executed.

One chip of the M50530-XXXFP can directly drive an 8-digit LCD for 1 line, 2 lines, and 4 lines. However, if a LCD with more digits is desired, it is necessary to connect an external IC for the LCD drive; either M50521FP or M50524FP. These ICs for LCD drive can drive a LCD as a common signal drive or column signal drive. Furthermore, when a large number of these ICs are used, the system is designed such that the data signals can be received only by the IC that is supplied with the chip select signal. This design allows the system can be operated with low power consumption.

The LCD contents are present for a prescribed frame time which is determined by the oscillation frequency, and the time is constant independent of the line number of the display, duty ratio, digit number of the display, and character font.

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TERMINAL DESCRIPTION

Pin	Name	I/O	Function
85/ μ c	Interface changeover signal	I	This is used as a signal for changing over the interface between μ c and μ p. It should be set to "1" for 8085 μ p and to "0" for μ c mode.
I/OC1	Input/output control signal	I	In the μ c mode, this is used as the control signal for sending an instruction from the μ c to the M50530-XXXFP, and is used as part of the instruction code. In the 8085 μ p mode, it is connected to the WR signal of the 8085 μ p.
I/OC2	Input/output control signal	I	In the μ c mode, this is used as the control signal for sending an instruction from the μ c to the M50530-XXXFP, and is used as part of the instruction code. In the 8085 μ p mode, it is connected to the IO/M signal of the 8085 μ p.
R/W	Write/read signal	I	In the μ c mode, this is used as the control signal for sending an instruction from the μ c to the M50530-XXXFP, and is used as part of the instruction code. It is set to "0" for write instruction and to "1" for read instruction. In the 8085 μ p mode, it is connected to the RD signal of the 8085 μ p.
EX	Instruction start signal	I	In the μ c mode, this is used as the signal for the μ c to cause the M50530-XXXFP to start the execution of an instruction. In the 8085 μ p mode, it is connected to the ALE signal of the 8085 μ p.
DB ₇ ~ DB ₄	Data bus	I/O	These represent the 4 upper lines of the 8 line data buses. They are in tri-state bidirectional mode which enables inputting as well as outputting. These are used for instruction data transfer between the M50530-XXXFP and the μ c or μ p. When interfacing with the μ c is 4 bits, the lower 4 bits data are also transferred by these 4 lines of data buses. The DB ₇ is also used for reading a busy flag.
DB ₃ ~ DB ₀	Data bus	I/O	These are the 4 lower lines of the 8 line data buses. They are in tri-state bidirectional mode which enables inputting as well as outputting. These are used for instruction data transfer between the M50530-XXXFP and the μ c or μ p. When interfacing with the μ c is 4 bits, these 4 lines are not used.
DST	Data set signal	O	Signal for setting serial data sent to the drive IC to a latch.
SCL	Shift clock signal	O	Clock for successively shifting a serial data set sent to drive IC.
FRM	Frame signal	O	Display frame signal. Used as a changeover signal for driving the liquid crystal by AC power.
CS	Chip select signal	O	Signal for selecting the column drive IC. Data will be transferred only to the drive IC to which this signal is supplied.
CMD	Common data signal	O	Common data signal to be sent to the common drive IC. Connected to chip select of the drive IC.
CLD	Column data signal	O	Column data signal to be sent to column drive IC. Sends a character pattern serially. Value "0" corresponds to non-selection while "1" corresponds to selection.
COM1~ COM32	LCD Common signal	O	Common signal for driving the scanning side of the liquid crystal. Common signals that are not used are all given the non-select waveform. For instance, if the duty is 1/16, then COM17 to COM32 will always be given non select waveforms.
COL1~ COL40	LCD Column signal	O	Column signal for driving the data side of the liquid crystal. Drives the respective 8-digit portion of the RAM display data of the display start address for each line.
OSC1, OSC2	Oscillation input/output	I/O	Terminal for oscillating internal clock. Connected to a resistor or a ceramic filter. Clock input from outside is supplied to OSC1.
V ₁ ~V ₅	Power supply(LCD)	I	Power supply for driving liquid crystal display. Voltages V _{SS} , V ₁ , V ₄ , and V ₅ are common while V _{SS} , V ₂ , V ₃ , and V ₅ are for column.
V _{DD}	Power supply(Logic)	I	Power supply for the logic circuit, +5V
V _{SS}	Power supply(GND)	I	Ground power supply, 0V

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FUNCTIONAL EXPLANATION OF EACH BLOCK

In the description below, the following abbreviations will be used:

Display data RAM : DD RAM

Character generator RAM : CG RAM

Character generator ROM : CG ROM

Display data/character generator RAM : DD/CG RAM

In addition, the designations of instructions will follow the abbreviations given in the instruction list. Use will also be made of the instruction code names in the instruction list.

The relationship between the binary logic values and the voltage levels is as given below.

Binary number 0 : Low voltage level

Binary number 1 : High voltage level

Furthermore, the following notations will be employed.

()_n means that the numerical value within the parentheses is that of the n-ary notation, namely, the number system in which n is used as the radix.

R()_n means the content of the RAM address ()_n.

It should be noted that unless otherwise stated, numerical values without suffix are meant for decimal notation.

For instance,

$(8F)_{16} \equiv (10001111)_2 \equiv (143)_{10} \equiv 143$, and

$R(8F)_{16} \equiv R(10001111)_2 \equiv R(143)$ means the content of the address 143 to the RAM.

1 INTERFACE CIRCUITS FOR μc AND μp

These are the circuits for controlling input and output when instructions and data are transferred between the M50530-XXXFP and external μc or μp that control the M50530-XXXFP.

By means of the input signal 85/ μc , it is possible to select either 8085 μp or μc as an external control.

When μc is selected, it is further possible to select 8-bit μc or 4-bit μc by the instruction SF. For the transfer of an instruction code from the 8-bit μc to the M50530-XXXFP, the input signals I/OC1, I/OC2, R/W, and the input/output signals DB₇ to DB₀, are used and the input signal EX are used for starting the execution of the instruction. For the transfer of an instruction code from the 4-bit μc to the M50530-XXXFP, the input signals I/OC1, I/OC2, R/W, and the input/output signals DB₇ to DB₄, are used twice. The input signal EX are also used twice for starting the execution of the instruction. In other words, in the 8-bit μc , the data buses DB₇ to DB₀ with 8 bits are used, and in the case of the 4-bit μc , the data buses DB₇ to DB₄ with 4 bits are used.

When the 8085 μp is selected, by connecting the signals AD₇ to AD₀, ALE, RD, WR, and IO/M of the 8085 μp to the signals DB₇ to DB₀, EX, R/W, I/OC1 and I/OC2, respectively, of the M50530-XXXFP, it is possible to control directly the M50530-XXXFP by producing an instruction code for M50530-XXXFP using the input/output instructions for 8085 μp .

The external μc and μp and the M50530-XXXFP operate asynchronously. Accordingly, there is no need for the inputs from the μc and μp to be synchronous with the internal clock of M50530-XXXFP. Furthermore, the handling of the interface for the signals from the external μc and μp , or the execution of the instructions from the μc and μp , will in no way affect the LCD processing within M50530-XXXFP. Therefore, no flickering will be generated in the display due to inputs from the μc and μp .

2 BUSY FLAG

When the M50530-XXXFP is executing an instruction, the busy flag will show (1)₂.

When the busy flag is at (1)₂, no instruction from the μp or μc will be accepted. Therefore, it is necessary to give an instruction to M50530-XXXFP after confirming that the busy flag is (0)₂.

However, the busy flag read instruction alone, RB, can always be used even when another instruction is being executed, and by using the instruction RB, the condition of the busy flag can be read from DB₇ and DB₃.

3 INSTRUCTION REGISTER AND MODE REGISTER

An instruction from the μp or μc enters the instruction register via the μc and μp interface circuits. The instruction is executed when its content has been decoded.

Among the included instructions are those which can set up the following modes.

Instruction SF : 8-bit/4-bit interface

5 × 8 dots / 5 × 12 dots font display line number, RAM region

Instruction SE : Cursor shift mode, display shift mode

Instruction SD : Display mode, blink mode

Instruction SU : Underline write mode

Instruction SB : Blink frequency

The mode register stores the information of these modes.

These modes are used as conditions for execution of the instructions.

4 INPUT REGISTER AND OUTPUT REGISTER

The input data is entered into the input data register by the write instructions WC, WS, WD, and WU, and is transferred to the interior upon execution of the instruction.

Output data is outputted from the output data register to the μp or μc by the read instructions RC, RS, and RD. The output data for these instructions is prepared beforehand in the output data register.

5 CURSOR ADDRESS REGISTER

This is the register for specifying the DD/CG RAM address. In order to write data into the RAM using the instruction WD, or read data from the RAM using the instruction RD, or

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add an underline to the RAM using instruction WU, it is necessary to set, beforehand, the address of the RAM in the cursor address register. With the instruction WC it is possible to set data in the cursor address register. Also the content of the cursor address register can be read using the instruction RC.

By incrementing (+1) or by decrementing (-1) the content of the cursor address register using the instruction MA, it is possible to shift the cursor address to the RAM in the upward or the downward direction.

After writing or reading the data using the instructions WD or RD and the entry mode has been specified by the instruction SE, the content of the cursor address register can be automatically incremented (+1) or decremented (-1) as shown in table 1.

Table 1. Instruction SE and cursor address

Instruction SE CSR CONDITION		Automatic INC/DEC of the Cursor Address
(W)	(R)	
0	0	No automatic inc or dec
0	1	Inc or dec after execution of instruction RD
1	0	Inc or dec after execution of instruction WD
1	1	Inc or dec after execution of instruction RD and WD

The increment and decrement of the cursor address register are executed within the display data region and the character generator region, respectively, of the RAM.

The Fig. 1 is an example (of 4 kinds of configurations) in which the RAM is divided into the display data region and

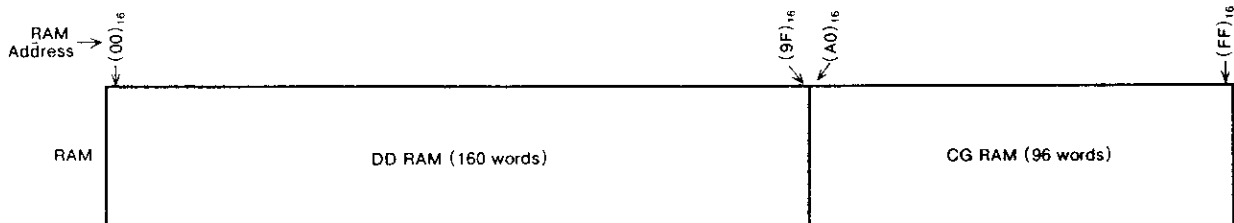


Fig.1 Example of dividing RAM

the character generation region. The increment and the decrement of the cursor address is as shown on the boundaries of the respective regions are as shown in table 2.

Table 2. Cursor Address

RAM Region	Cursor Address		
	Before inc/dec	After inc	After dec
DD RAM	(00) ₁₆	(01) ₁₆	(9F) ₁₆
	(9F) ₁₆	(00) ₁₆	(9E) ₁₆
CG RAM	(A0) ₁₆	(A1) ₁₆	(FF) ₁₆
	(FF) ₁₆	(A0) ₁₆	(FE) ₁₆

The boundary conditions in the increment and the decrement of the cursor address are displayed in 2 lined and 4 lines so that the conditions will remain the same as in the above table even when the RAM region is further subdivided.

6 DISPLAY START ADDRESS REGISTER

This is the register for determining the relative relationship between the position of the displayed character in the LCD and the address of the DD RAM in which the character is written.

The content of the display start address register designates the address of the RAM in which the character code of the character to be displayed in the first digit on the left end of the LCD.

The range of the display start address varies with the size of the RAM region and the number of displayed lines.

In the case of 2-line display, the display start addressed for

the first line and the second line have a common value, and in the case of 4-line display, the display start addresses for the first through fourth lines have a common value. In the case of display of more than 2 lines, the value of the display start address of the first line is used as the value of the display start address. Accordingly, the range of the display start address is given depending upon the size of the RAM region and the number of display lines, as table 3.

Table 3. Range of display start address

Instruction SF		DD RAM Region	Range of Display Start Address		
RA ₁	RA ₀		1-line Display	2-line Display	4-line Display
0	0	256 words (00) ₁₆ ~(FF) ₁₆	(00) ₁₆ ~(FF) ₁₆	(00) ₁₆ ~(7F) ₁₆	(00) ₁₆ ~(3F) ₁₆
0	1	224 words (00) ₁₆ ~(DF) ₁₆	(00) ₁₆ ~(DF) ₁₆	(00) ₁₆ ~(6F) ₁₆	(00) ₁₆ ~(37) ₁₆
1	0	192 words (00) ₁₆ ~(BF) ₁₆	(00) ₁₆ ~(BF) ₁₆	(00) ₁₆ ~(5F) ₁₆	(00) ₁₆ ~(2F) ₁₆
1	1	160 words (00) ₁₆ ~(9F) ₁₆	(00) ₁₆ ~(9F) ₁₆	(00) ₁₆ ~(4F) ₁₆	(00) ₁₆ ~(27) ₁₆

By setting a display start address in the display start address register with the instruction WS, it is possible to display starting with the first digit of the LCD, from an arbitrary address of the DD RAM.

The content of the display start address register can be read with the instruction RS.

By incrementing (+1) or decrementing (-1) the content of the display start address register with the instruction MA, the position of the liquid crystal display with respect to the

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RAM can be shifted upward or downward.

After writing or reading the data with the instruction WD or RD, it is possible to automatically increment (+1) or decrement (-1) the content of the display start address register by designating the entry mode with the instruction SE. This is shown in table 4.

Table 4. Instruction SE and display start address

Instruction SE DSP CONDITION		Automatic inc/dec of Display Start Address
(W)	(R)	
0	0	No automatic inc or dec
0	1	Inc or dec after execution of the instruction RD
1	0	Inc or dec after execution of the instruction WD
1	1	Inc or dec after execution of the instructions RD and WD

The increment and the decrement of the content of the display start address register are executed within the data region for the first line in the display data region of the RAM. The relation between the RAM address and the content of the display start address register will now be explained, when the RAM is divided into 160 words of DD RAM and 96 words of the CG RAM (one of the 4 possible configurations).

An example of the case of 1-line of LCD (for 160 words of DD RAM and 96 words of CG RAM) ; Fig. 2.

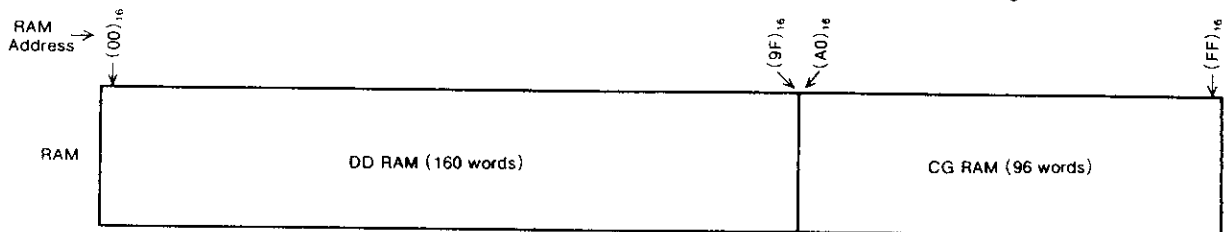


Fig.2 DD/CG RAM

When the content of the display start address register is (17)₁₆, the liquid crystal display will be as Fig. 3.

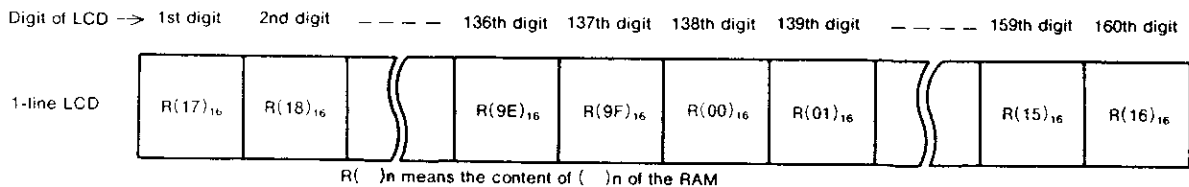


Fig.3 Example of display address

Here, if the content of the display start address register is incremented (+1), the result becomes (18)₁₆, and the LCD display will be given by Fig. 4.

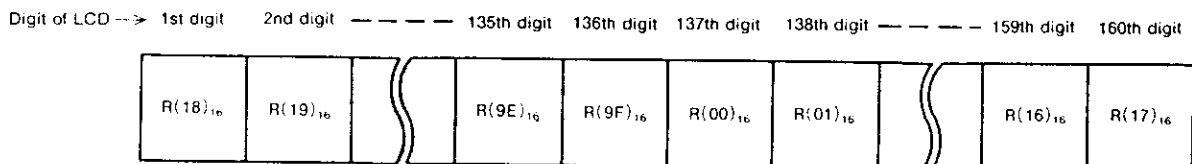


Fig.4 Example of display address

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Visually, the content of the displayed content looks as if it is shifted to the left. Similarly, when the content of the display start address register is decremented, the displayed content looks as if it is shifted to the right. When the display

start address is situated on the boundary of the display data region of the RAM, if the display start address is incremented or decremented, the result will be as shown in table 5.

Table 5. Change of display start address

Display Start Address		
Before inc/dec	After inc	After dec
(00) ₁₆	(01) ₁₆	(9F) ₁₆
(9F) ₁₆	(00) ₁₆	(9E) ₁₆

An example of the case of 2-line of LCD (for 160 words of DD RAM and 96 words of CG RAM) ; Fig. 5.

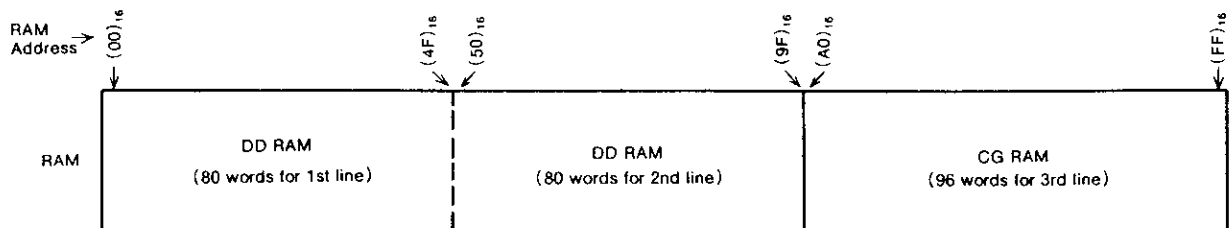


Fig.5 DD/CG RAM

When the content of the display start address register is (17)₁₆, the LCD is given by Fig. 6.

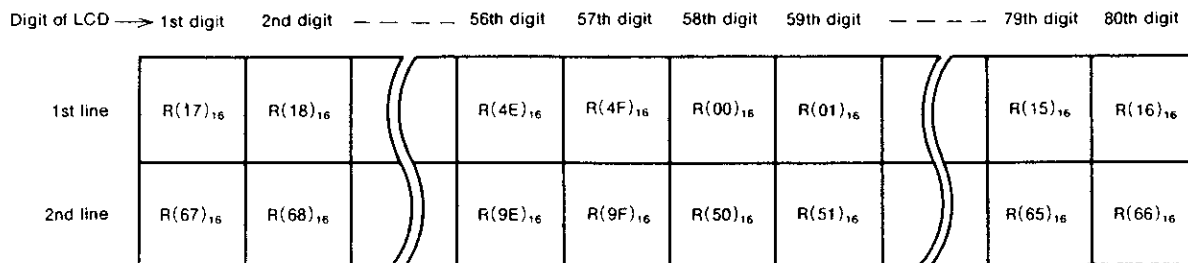


Fig.6 Example of display address

When the content of the display start address register is incremented, the result becomes (18)₁₆, and the LCD becomes as shown in Fig. 7

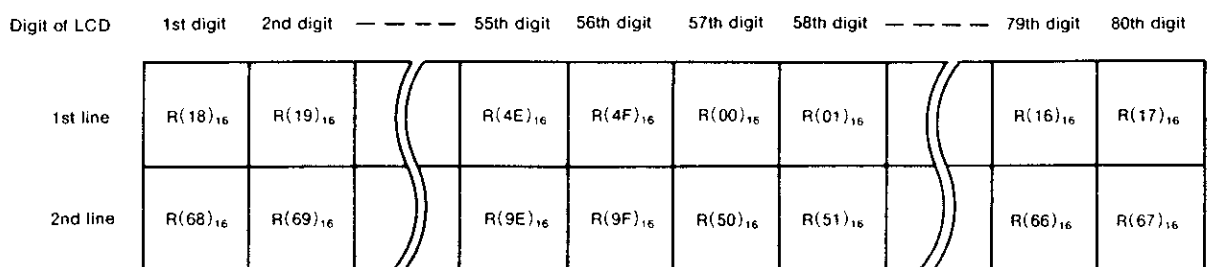


Fig.7 Example of display address

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The displayed contents of the first and the second lines look visually as if they are simultaneously shifted to the left. Similarly, if the content of the display start address register is decremented, the displayed contents of the first and the second lines look as if they are shifted simultaneously to

the right. When the display start address is situated on the boundary of the display data region of the first line of the RAM, by incrementing or decrementing the display start address the result becomes as shown in table. 6.

Table 6. Change of display start address

Display Start Address		
Before inc/dec	After inc	After dec
(00) ₁₆	(01) ₁₆	(4F) ₁₆
(4F) ₁₆	(00) ₁₆	(4E) ₁₆

Case of 4-line LCD (for 160 words of DD RAM and 96 words of CG RAM) ; Fig. 8.

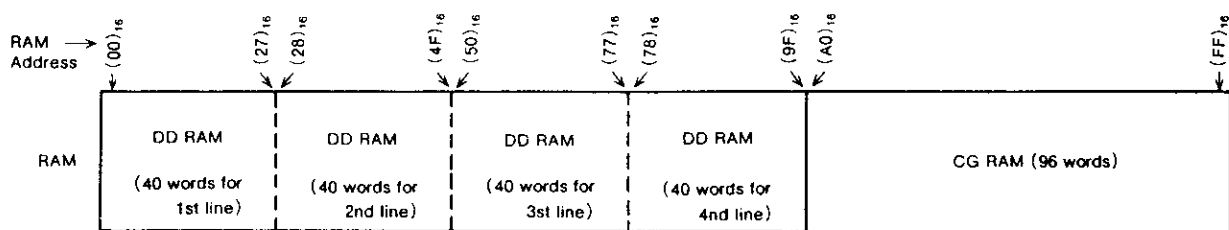


Fig.8 DD/CG RAM

When the content of the display address register is (17)₁₆,

LCD will be as Fig. 9:

Digit of LCD → 1st digit 2nd digit ——— 16th digit 17th digit 18th digit 19th digit ——— 39th digit 40th digit

1st line	R(17) ₁₆	R(18) ₁₆		R(26) ₁₆	R(27) ₁₆	R(00) ₁₆	R(01) ₁₆		R(15) ₁₆	R(16) ₁₆
2nd line	R(3F) ₁₆	R(40) ₁₆		R(4E) ₁₆	R(4F) ₁₆	R(28) ₁₆	R(29) ₁₆		R(3D) ₁₆	R(3E) ₁₆
3rd line	R(67) ₁₆	R(68) ₁₆		R(76) ₁₆	R(77) ₁₆	R(50) ₁₆	R(51) ₁₆		R(65) ₁₆	R(66) ₁₆
4th line	R(8F) ₁₆	R(90) ₁₆		R(9E) ₁₆	R(9F) ₁₆	R(78) ₁₆	R(79) ₁₆		R(8D) ₁₆	R(8E) ₁₆

Fig.9 Example of display address

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When the content of the display start address register is incremented, the result is $(18)_{16}$, and the LCD will be given by Fig. 10

Digit of LCD → 1st digit 2nd digit — — — — 15th digit 16th digit 17th digit 18th digit — — — — 39th digit 40th digit

1st line	$R(18)_{16}$	$R(19)_{16}$		$R(26)_{16}$	$R(27)_{16}$	$R(00)_{16}$	$R(01)_{16}$		$R(16)_{16}$	$R(17)_{16}$
2st line	$R(40)_{16}$	$R(41)_{16}$		$R(4E)_{16}$	$R(4F)_{16}$	$R(28)_{16}$	$R(29)_{16}$		$R(3E)_{16}$	$R(3F)_{16}$
3st line	$R(68)_{16}$	$R(69)_{16}$		$R(76)_{16}$	$R(77)_{16}$	$R(50)_{16}$	$R(51)_{16}$		$R(66)_{16}$	$R(67)_{16}$
4th line	$R(90)_{16}$	$R(91)_{16}$		$R(9E)_{16}$	$R(9F)_{16}$	$R(78)_{16}$	$R(79)_{16}$		$R(8E)_{16}$	$R(8F)_{16}$

Fig.10 Example of display address

The displayed content of the first, second, third and fourth lines look visually as if they are shifted simultaneously to the left. Similarly, if the content of the display start address register is decremented, the displayed contents of the first, second, third and fourth lines look as if they are shifted simultaneously to the right. When the display start address is situated on the boundary of the display data region of the first line of the RAM, if the display start address is incremented or decremented, the result will be given by table 7

Table 7. Change of display start address

Display Start Address		
Before inc/dec	After inc	After dec
$(00)_{16}$	$(01)_{16}$	$(27)_{16}$
$(27)_{16}$	$(00)_{16}$	$(26)_{16}$

7 DISPLAY ADDRESS REGISTER

This is the register for designating the address of a displayed data of the RAM to be displayed by the liquid crystal.

To read all of the displayed data of the RAM during the times for the respective common signals, convert them to a character pattern, and transfer them to the column driver; the content of the display address register is continuously and successively changed from the display start address, and the RAM address is scanned and designated.

8 ADDRESS DATA CONTROL

This is to execute display processing, instruction processing, and more for the address and data of the RAM and the ROM by controlling the cursor address register, display start address register, display address register, and so forth.

9 DISPLAY DATA/CHARACTER GENERATOR RAM (DD/CG RAM)

This is the RAM for storing the data and the character fonts for the character generator to be displayed by the liquid crystal. There are altogether 256 words, each word consisting of 9 bits. The 256 word RAM can be divided into a region to be used for display data (DD RAM) and a region to be used by the character generator (CG RAM). The division of the RAM into the DD RAM and the CG RAM is carried out by the instruction SF, and there are 4 kinds of divisions (table 8):

Table 8. Instruction SF and RAM word number

Instruction SF		RAM Word Number(9bits for a word)	
RAM		DD RAM	CG RAM
RA_1	RA_0		
0	0	256 words	0 words
0	1	224 words	32 words
1	0	192 words	64 words
1	1	160 words	96 words

9-1 Display Data RAM (DD RAM)

When 9 bits of a word in the RAM are used as a display data, 8 bits are used for display character code and the remaining 1 bit is used for underline display.

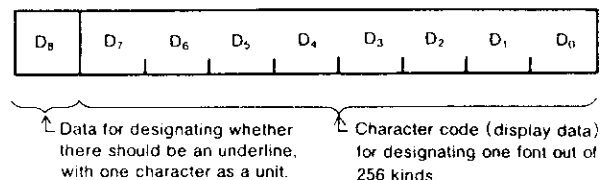


Fig.11 RAM data.

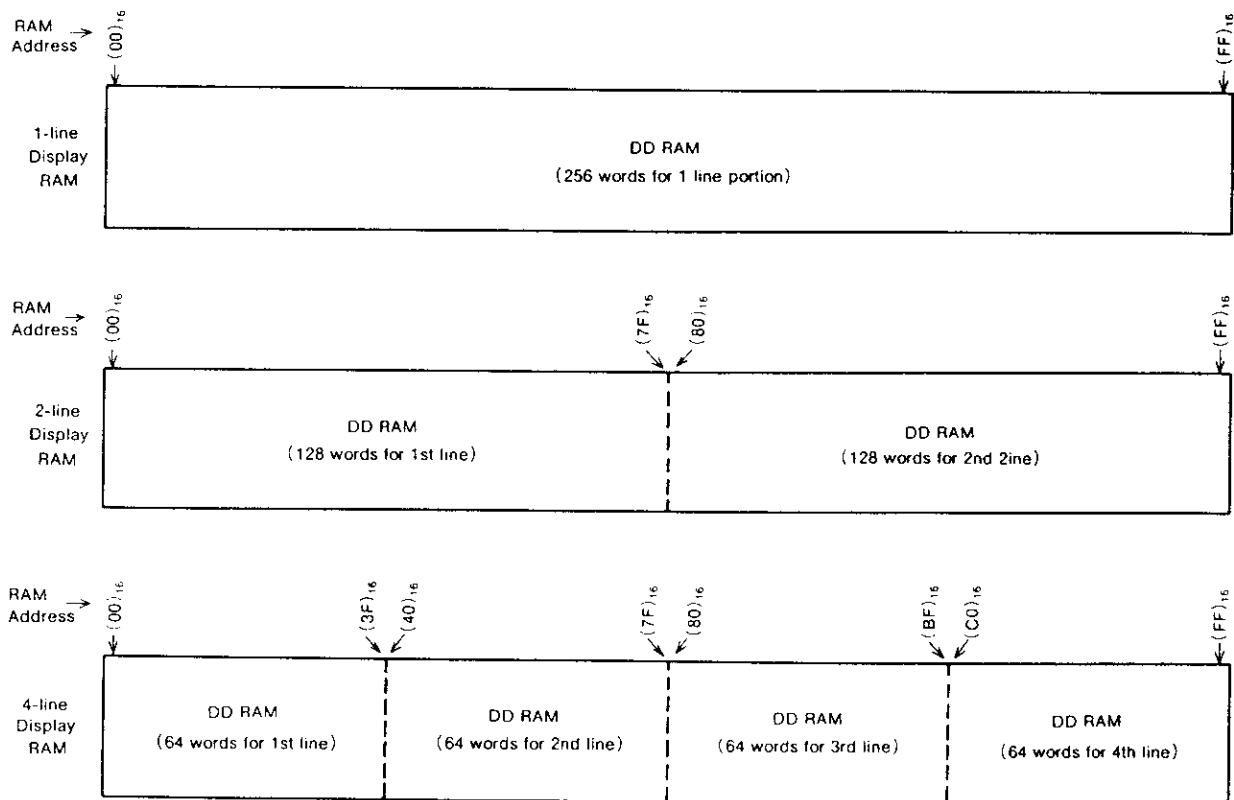
DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

The DD RAM is given the composition of table 9 by the duty which designates one of 1-line display, 2-line display, and 4-line display, and the font setting instruction SF. Next, the addresses for each display line of the DD RAM and the addresses of the CG RAM will be shown in the diagram (9-1-1 ~ 9-1-4) for each of these 4 kinds of RAM composition.

Table 9. Instruction SF and RAM composition

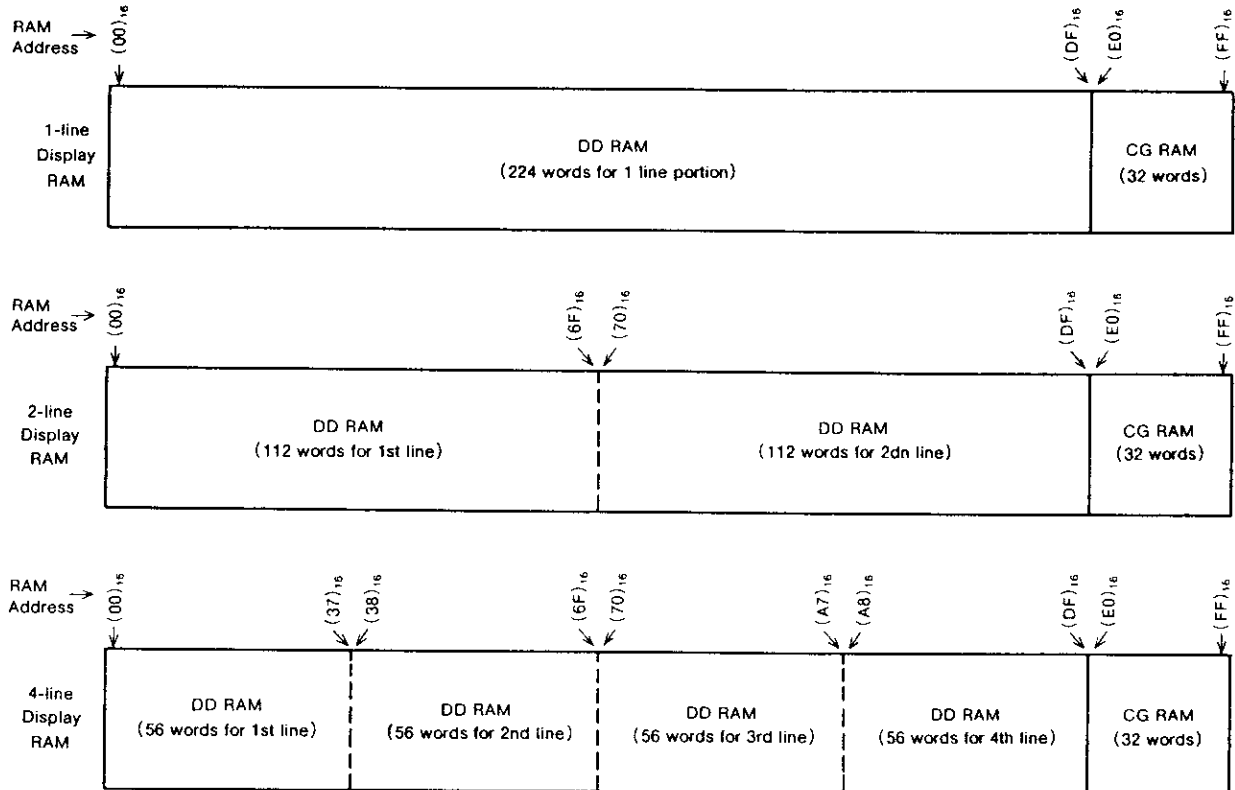
		1-line Display		2-line Display		4-line Display		
Instru- ction SF	Font	1	Duty 1/8		Duty 1/16		Duty 1/32	
	8/12	0	Duty 1/12		Duty 1/24		Duty 1/48	
			DT ₁	0		0		1
			D _{T0}	0		1		0
RA ₁	RA ₀		0		1		0	
0	0	1 line×256 words		2 line×128 words		4 line× 64 words		
0	1	1 line×224 words		2 line×112 words		4 line× 56 words		
1	0	1 line×192 words		2 line× 96 words		4 line× 48 words		
1	1	1 line×160 words		2 line× 80 words		4 line× 40 words		

9-1-1 Case of 256 words for DD RAM and 0 word for CG RAM

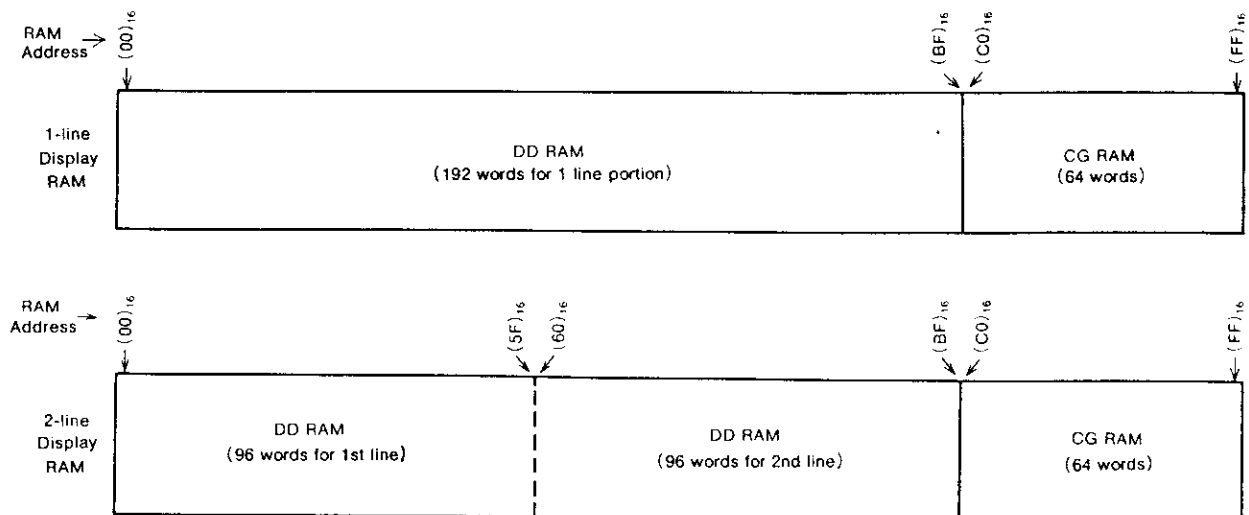


DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

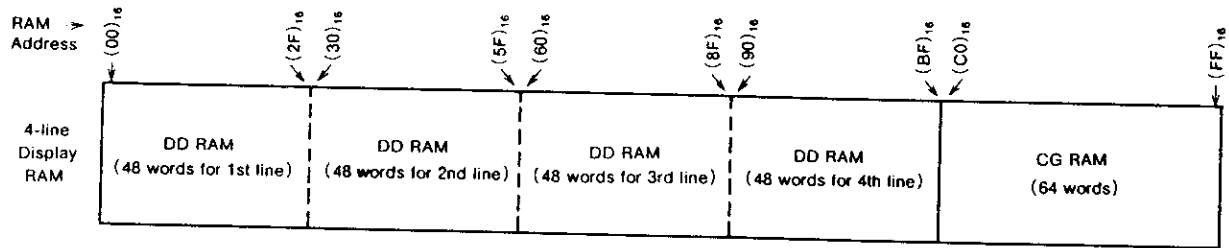
9-1-2 Case of 224 words for DD RAM and 32 words for CG RAM



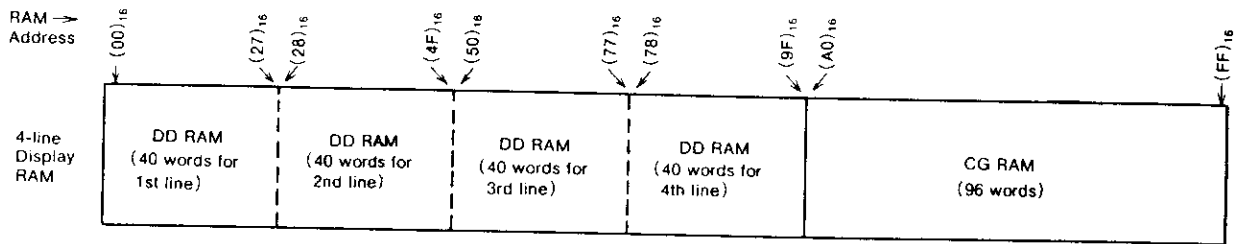
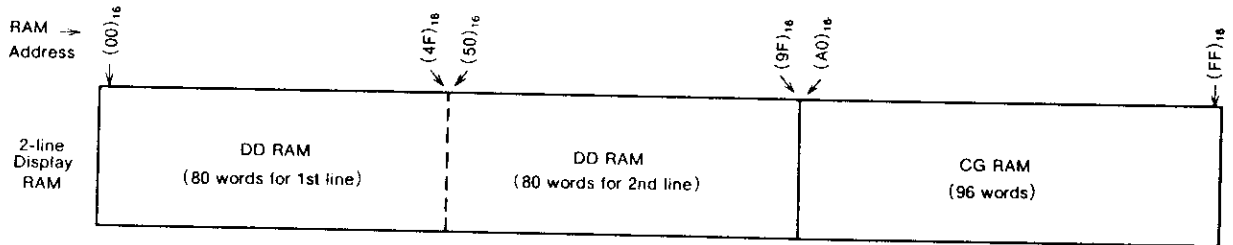
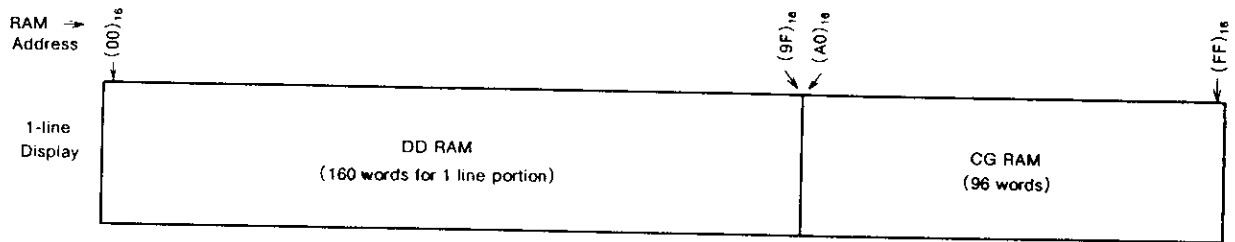
9-1-3 Case of 192 words for DD RAM and 64 words for CG RAM



DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER



9-1-4 Case of 160 words for DD RAM and 96 words for CG RAM



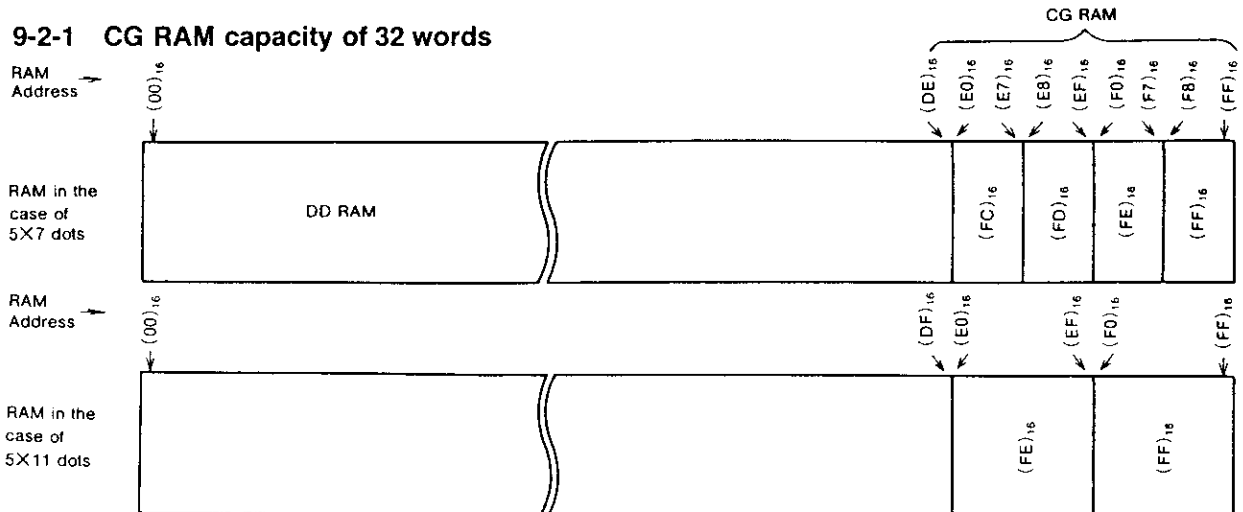
DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

9-2 Character Generator RAM (CG RAM)

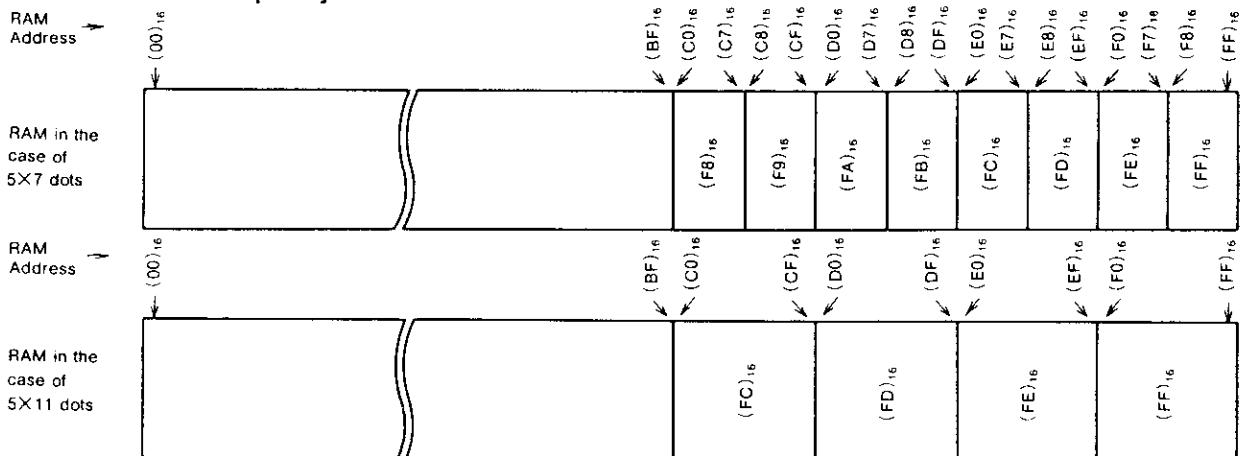
In the CG RAM the user can write an arbitrary font of 5X7 dots or 5X11 dots. A maximum of 12 character fonts in the case of 5X7 dots, and a maximum of 6 fonts in the case of 5X11 dots, can be written in the CG RAM.

The address of the CG RAM which is written a character font and the character code of the character font are made to correspond in a 1 to 1 fashion as shown in the diagram (9-2-1~9-2-4).

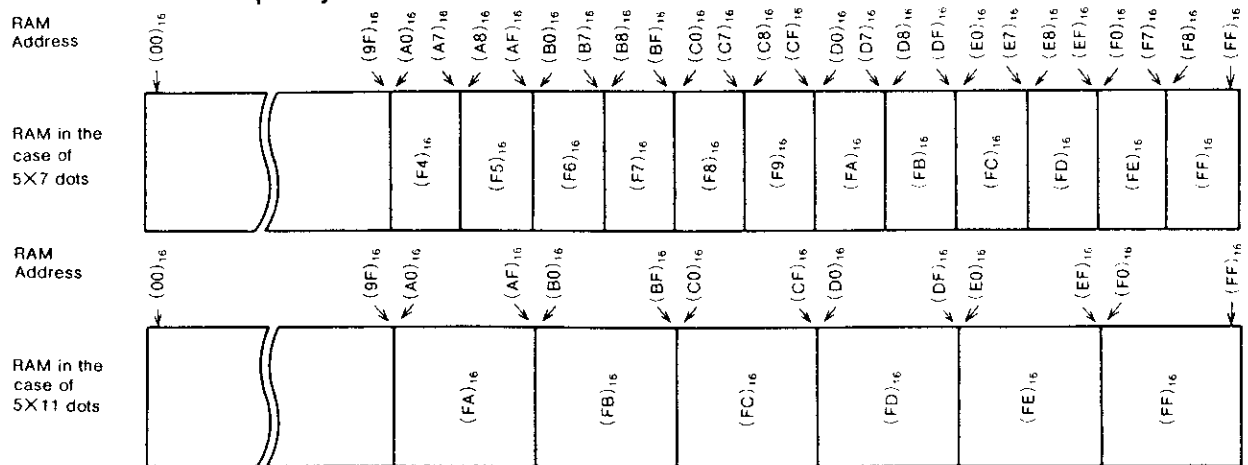
9-2-1 CG RAM capacity of 32 words



9-2-2 CG RAM capacity of 64 words



9-2-3 CG RAM capacity of 96 words



DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

Next, an example of constructing a character font from an address and a data of the CG RAM for each character code will be described.

CHARACTER FONT OF 5X7 DOTS

Example for
character code $(FE)_{16}$

CG RAM upper
addresses determined
by character code

Example for
character code $(FF)_{16}$

CG RAM Address							
A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
					0	0	0
					0	0	1
					0	1	0
					0	1	1
1	1	1	1	0	1	0	0
					1	0	1
					1	1	0
					1	1	1
					0	0	0
					0	0	1
					0	1	0
					0	1	1
1	1	1	1	1	1	0	0
					1	0	1
					1	1	0
					1	1	1

CG RAM Data							
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
			0	0	1	0	0
			0	1	0	0	0
			1	0	0	0	1
			1	0	0	0	1
			1	1	1	1	1
			1	0	0	0	1
			1	0	0	0	1
			1	0	0	0	1
			1	1	1	1	0
			0	1	0	0	1
			0	1	0	0	1
			0	1	0	0	1
			0	1	0	0	1
			1	1	1	1	0

Example for character
pattern "A"

Example for character
pattern "B"

The portion of the CG RAM marked with an "*", namely, data D₇ D₆ D₅ and data D₇~D₀ in which the address for A₂ A₁ A₀ is $(111)_2$, will not be used as a pattern for a character font. However, it can be used for general data RAM.

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

CHARACTER FONT OF 5X11 DOTS

		CG RAM Address								CG RAM Data							
		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Example for character code (FE) ₁₆	1 1 1 0					0	0	0	0	0	0	1	1	0			
						0	0	0	1	0	1	0	0	0	1		
						0	0	1	0	1	0	0	0	0	1		
						0	0	1	1	1	0	0	0	0	1		
						0	1	0	0	1	0	0	0	0	1		
						1	0	1	0	1	0	0	0	0	1		
						0	1	1	0	1	0	0	0	0	1		
						0	1	1	1	1	0	0	0	0	1		
						1	0	0	0	1	0	0	0	0	1		
						1	0	0	1	1	0	0	0	0	1		
						1	0	1	1	1	0	0	0	0	1		
						1	1	0	0	1	0	0	0	0	1		
						1	1	1	0	1	0	0	0	0	1		
						1	1	1	1	1	0	0	0	0	1		
						0	0	0	0	0	1	1	1	1	1		
						0	0	0	1	1	0	0	0	0	0		
CG RAM upper addresses determined by character code	1 1 1 1					0	0	1	0	0	1	1	1	0			
						0	0	1	1	0	0	0	0	0	1		
						0	1	0	0	1	0	0	0	0	1		
						0	1	0	1	1	0	0	0	0	1		
						0	1	1	0	1	0	0	0	0	1		
						0	1	1	1	1	0	0	0	0	1		
						1	0	0	0	1	0	0	0	0	1		
						1	0	1	0	1	0	0	0	0	1		
						1	0	1	1	1	0	0	0	0	1		
						1	1	0	0	1	0	0	0	0	1		
						1	1	0	1	1	0	0	0	0	1		
						1	1	1	0	1	0	0	0	0	1		
						1	1	1	1	1	0	0	0	0	1		
						0	0	0	0	0	1	1	1	1	1		
						0	0	0	1	1	0	0	0	0	0		
						0	0	0	0	1	1	1	1	1	0		
Example for character code (FF) ₁₆	1 1 1 1					0	0	0	0	0	1	1	1	1	0		
						0	0	0	1	1	0	0	0	0	1		
						0	0	0	1	1	0	0	0	0	1		
						0	1	0	0	1	0	0	0	0	1		
						0	1	0	1	1	0	0	0	0	1		
						0	1	1	0	1	0	0	0	0	1		
						0	1	1	1	1	0	0	0	0	1		
						1	0	0	0	1	0	0	0	0	1		
						1	0	1	0	1	0	0	0	0	1		
						1	0	1	1	1	0	0	0	0	1		
						1	1	0	0	1	0	0	0	0	1		
						1	1	0	1	1	0	0	0	0	1		
						1	1	1	0	1	0	0	0	0	1		
						1	1	1	1	1	0	0	0	0	1		
						0	0	0	0	0	1	1	1	1	1		
						0	0	0	1	1	0	0	0	0	0		

The portion marked with an "*", namely data D₇ D₆ D₅ and data D₇ ~ D₀ in which the address A₃ A₂ A₁ A₀ is in the range from (1011)₂ to (1111)₂, will not be used as a pattern for character font. However, it can be used for general data RAM.

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

To write and read character pattern data for character font from the CG RAM, the address is set in the cursor address register with the instruction WC, analogous to the case of writing and reading a data from the DD RAM. Writing and reading are executed with the instructions WD and RD using 8 bits per word. Of the 8 bits in a word 5 bits are made to correspond to 5 dots in a line as character pattern data for the character font. The bits of the CG RAM data, $(1)_2$ corresponds to the display selection by the LCD dots while $(0)_2$ corresponds to the nondisplay selection. In the case of a character font of 5×7 dots, the bit is written 7 words for 7 line portions, and in the case of a character font of 5×11 dots, it is necessary to write the bit for 11 words for 11 line portions.

10 CHARACTER GENERATOR ROM (CG ROM)

This is the ROM for generating a fixed character font from the character codes with display data 8 bits. The content of CG ROM (character fonts) is programable by mask ROM. 256 kinds of character fonts of 5×7 dots or 5×11 dots as dot-matrix characters can be stored.

These 256 kinds of font represent the sum of the number of the character fonts generated in the CG RAM and the number of the character fonts generated in the CG ROM. Accordingly, the number of fonts that can be generated in the CG RAM and the CG ROM varies depending upon the division ratio of the DD RAM and the CG RAM regions and also upon whether using 5×7 dots or 5×11 dots. Those combinations are shown in table 10.

The relationship between the range of the character codes corresponding to the CG RAM and the range of the character codes corresponding to the CG ROM will now be shown.

Of the character codes, the space code is a special code which is used for the clear display. All of the dot bits in the character font 5×11 dots for the CG ROM content that correspond to the space code are $(0)_2$, indicating nondisplay. And the space code must be set up between from character code $(00)_{16}$ to $(F3)_{16}$.

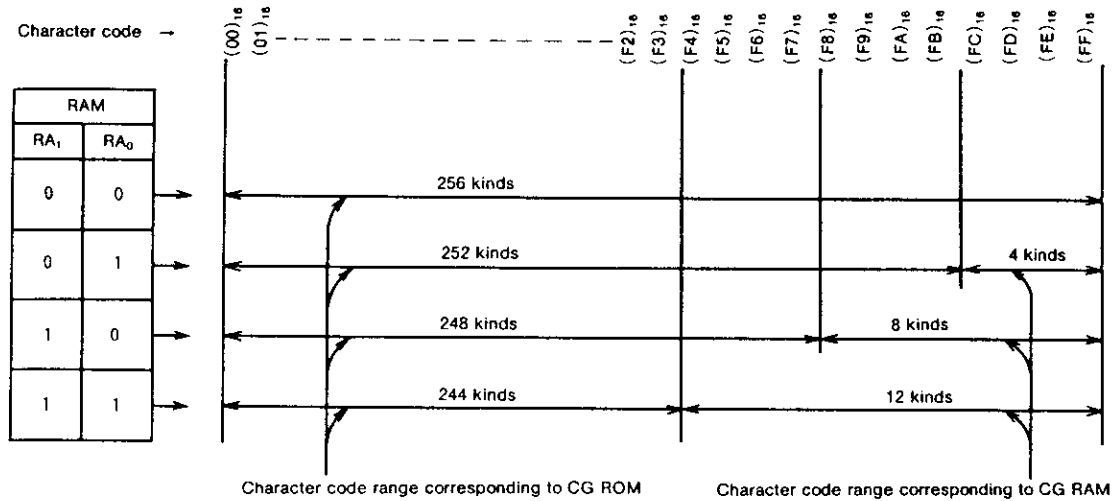
When the DD RAM content is cleared by the autoclear or the instruction CH, all of the display data go to the space code.

Table 10. Display font number

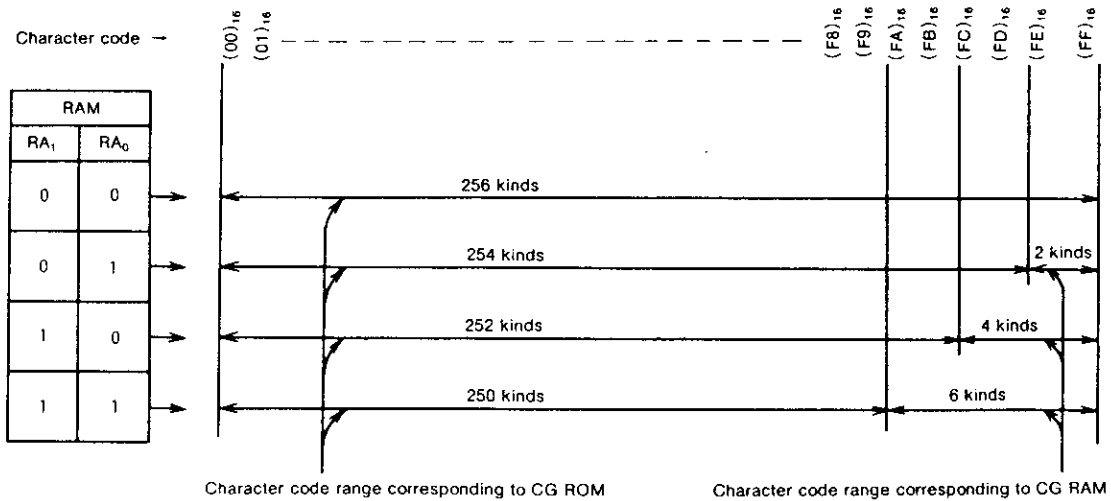
Dot Matrix Composition	Instruction SF		CG RAM			CG ROM
	Font B/12	RA ₁	RA ₀	Memory Capacity(words)	Font Number(kinds)	Font Number(kinds)
5×7 dots	1	0	0	0	0	256
		0	1	32	4	252
		1	0	64	8	248
		1	1	96	12	244
5×11 dots	0	0	0	0	0	256
		0	1	32	2	254
		1	0	64	4	252
		1	1	96	6	250

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

CASE OF CHARACTER FONT OF
5×7 DOTS



CASE OF CHARACTER FONT OF
5×11 DOTS



DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

11 SERIES/PARALLEL CONVERSION CIRCUIT

This is the circuit for sending a parallel font pattern data from the CG ROM or the CG RAM to the column driver by converting it to a serial data.

12 DISPLAY, CURSOR, AND BLINK CONTROLS

They control the ON/OFF of the LCD, cursor display, blinking display, and so forth. Various display modes given below can be set using the instruction SD.

- ON/OFF of the entire display
- ON/OFF of the cursor
- ON/OFF of the underline display
- Blinking of the cursor display
- Blinking of a character at the cursor position

By the use of the instruction SB, 1 blinking frequency can be selected out of the following 4 kinds.

0.5Hz 1Hz 2Hz 4Hz

(for an oscillation frequency of about 2.5MHz)

The cursor will be displayed on the lowest line of the font matrix as indicated below.

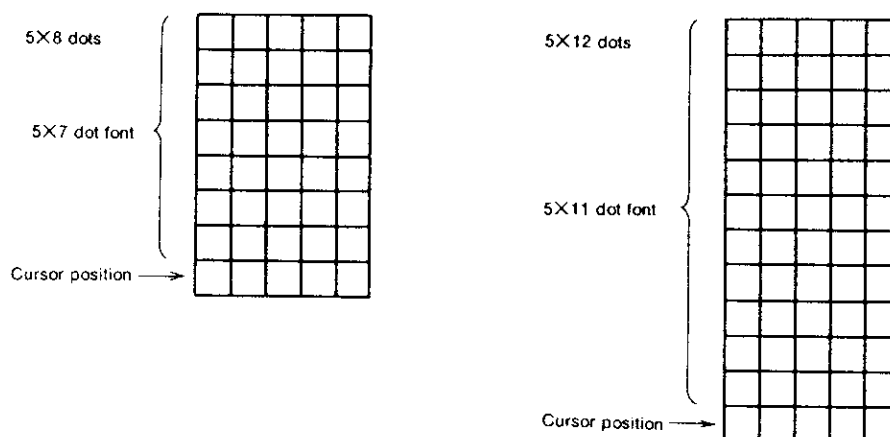


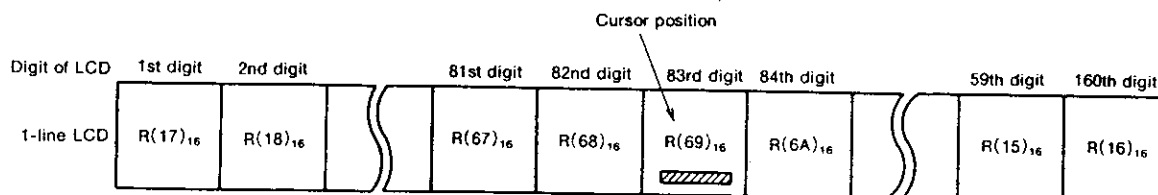
Fig.12. Position of character font and cursor.

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

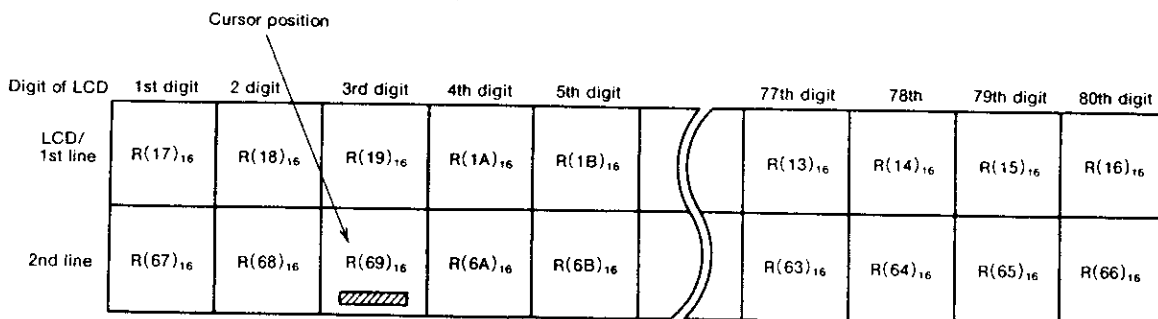
The cursor display and the blinking display will be displayed at the digit position of the RAM display data which is designated by the cursor address register.

When the content of the cursor register is $(69)_{16}$ and the content of the display start register is $(17)_{16}$, the display positions of the cursor and the blinking are as shown below.

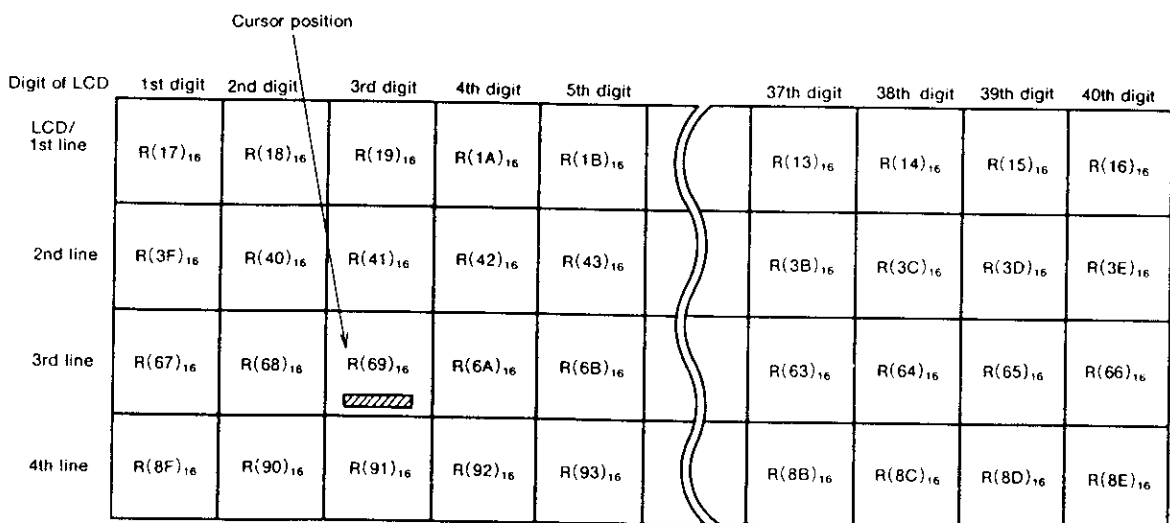
- 1 line of LCD (for 160 words of DD RAM and 96 words of CG RAM)



- 2 lines of LCD (same conditions as above)



- 4 lines of LCD (same conditions as above)



DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

13 COMMON SIGNAL OUTPUT CIRCUIT

There are 32 lines of common signal drive output which directly drive the common side of the LCD.

Therefore, it is possible to directly drive the common signals with the display duties ranging from 1/8 to 1/32. Further, by connecting a common driver for expansion, M50521FP or M50524FP in the outside, it becomes possible to drive common signals up to a duty of 1/48. The output signal CMD is the common signal to be sent to the external common driver.

The unused common drive outputs become nondisplay selection signals. For example, when duty is 1/16, the common outputs COM1~COM16 output common scanning signals, but COM17~COM32 always output nondisplay selection signals.

The instruction SF can set the character font and the duty, and the number of display lines and the effective common signal are given as shown in the Table. 11.

14 COLUMN SIGNAL OUTPUT CIRCUIT

The display data which is converted to a character font pattern is sent to a 40-bit shift register as serial pattern data, and is then latched.

The latched output controls the driver to output 40 lines of column signals that directly drive the liquid crystal display.

With the 40 lines of column signals it is possible to directly drive an 8 digit portion LCD for either a 1-line, 2-line, or 4-line display.

The number of displayed digits can be expanded by transferring the character font pattern data to an external column driver (M50521FP or M50524FP) from the column data output signal CLD. Depending upon the number of bits of the column driver (which is connected externally) it is possible to expand the character display from an arbitrary digit number to a maximum digit number.

15 TIMING SIGNAL GENERATING CIRCUIT

The oscillation circuit generates various kinds of internal timing signals to be used for display processing, instruction processing, and so forth.

In addition, the circuit generates timing signals for controlling the external LCD driver in order to expand the digit number of the LCD.

The processing of an instruction is executed totally independently of the LCD processing so that there will be no change in the processing time of LCD which is determined by the duty employed.

Further, the period for liquid crystal to display all of the display patterns once, (the period of the common signal) depends only on the oscillation frequency. The period of the cursor/character display blinking, also depends only on the oscillation frequency.

Table 11. Effective common signal output

Character Font	Instruction SF			Duty	Number of Display Lines	Effective Common Signal Output
	Font 8/12	DT ₁	DT ₀			
5 X 8 dots	1	0	0	1/8	1	COM1~COM8
		0	1	1/16	2	COM1~COM16
		1	0	1/32	4	COM1~COM32
5 X 12 dots	0	0	0	1/12	1	COM1~COM12
		0	1	1/24	2	COM1~COM24
		1	0	1/48	4	*COM1~COM32

* By the use of an external common driver for expansion COM33~COM48 can be generated.

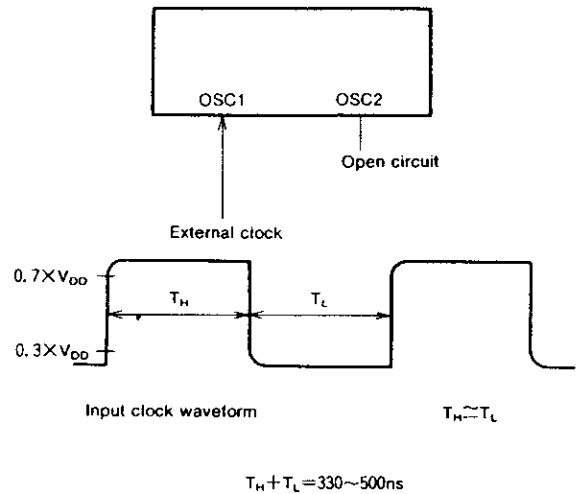
DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

16 OSCILLATOR

To generate an internal clock, it is possible to let the built-in oscillator induce self-oscillation by connecting a simple external part. It is also possible to input a clock to the oscillator from the outside.

16-1 Using an external clock

Input the external clock to the oscillator input terminal OSC1, and leave the oscillator output terminal OSC2 disconnected.



16-2 Using built-in oscillator

(16-2-1) The built-in oscillator can be set to oscillate by connecting an external resistor for oscillation between the terminals OSC1 and OSC2.

Try to minimize the wire length for connecting the resistor in order to reduce the external capacitance to be connected to the terminals OSC1 and OSC2.

(16-2-2) It is possible to set the built-in oscillator into oscillation by connecting a ceramic vibrator between the terminals OSC1 and OSC2 as in the figure.

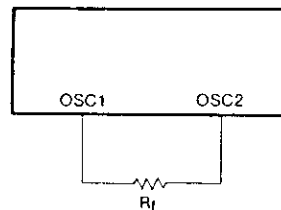
Next, the oscillation frequency of the oscillator and the period of the common signal are related by the following equations:

$$T_{COM} = \frac{36864}{f_{OSC}} \quad \text{Here, } T_{COM} : \text{Period of common signal (s)}$$

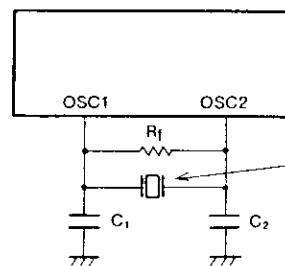
$$f_{COM} = \frac{1}{T_{COM}} \quad f_{COM} : \text{Inverse of } T_{COM} \text{ (Hz)}$$

$$f_{COM} = \frac{f_{OSC}}{36864} \quad f_{OSC} : \text{Oscillation frequency (Hz)}$$

For example, to obtain 70Hz for f_{COM} , f_{OSC} must be about 2.58MHz.



When the oscillation frequency is about 2.5 MHz,
 $R_f = 3.9K\Omega \pm 2\%$
 (Reference value)



Reference value
 ($f_{OSC} = 2.5\text{MHz}$)
 $R_f = 1M\Omega \pm 10\%$
 $C_1 = 100 \sim 220\text{pF}$
 $C_2 = 100 \sim 220\text{pF}$
 Ceramic vibrator: CSA 2.500MK
 (Made by Murata Corp.)

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

17 AUTOCLEAR

After closing the power supply, a built-in autoclear circuit is actuated to initialize RAM and various kinds of mode flags. While the autoclear is in operation, the busy flag is set to $(1)_2$.

- All of the 8bit display data of the RAM display data region are set to the space code, and all of the underline bits are set to $(0)_2$ (nondisplaying)
- The display start address and the cursor address are set to $(00)_{16}$.
- The mode flags to be used for the instructions are initial-

ized as Fig. 13

To operate the autoclear circuit without failure please be sure to let the power supply V_{DD} satisfy the conditions indicated in Fig. 14. When these conditions are not fulfilled, it is necessary to meet the conditions by the execution of instructions.

Function mode
(Instruction SF)

I/OC	FONT	DUTY		RAM	
8/4	8/12	DT ₁	DT ₀	RA ₁	RA ₀
1	0	0	0	0	0

Entry mode
(Instruction SE)

CSR	CSR CONDITION		DSP	DSP CONDITION	
D/I	W	R	D/I	W	R
0	0	0	0	0	0

Display mode
(Instruction SD)

DSP	CSR	UND	CSR	CHR
ON/OFF	ON/OFF	ON/OFF	BLINK	BLINK
0	0	0	1	1

Underline mode
(Instruction SU)

USR	UND
ON/OFF	S/R
0	1

Blinking mode
(Instruction SB)

BLINK FREQ	
B ₁	B ₀
0	1

Fig.13 Mode of initialization

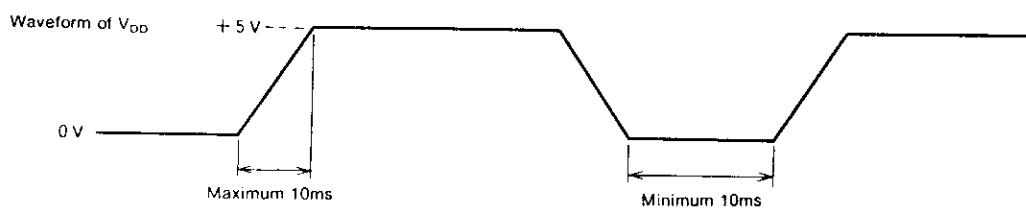
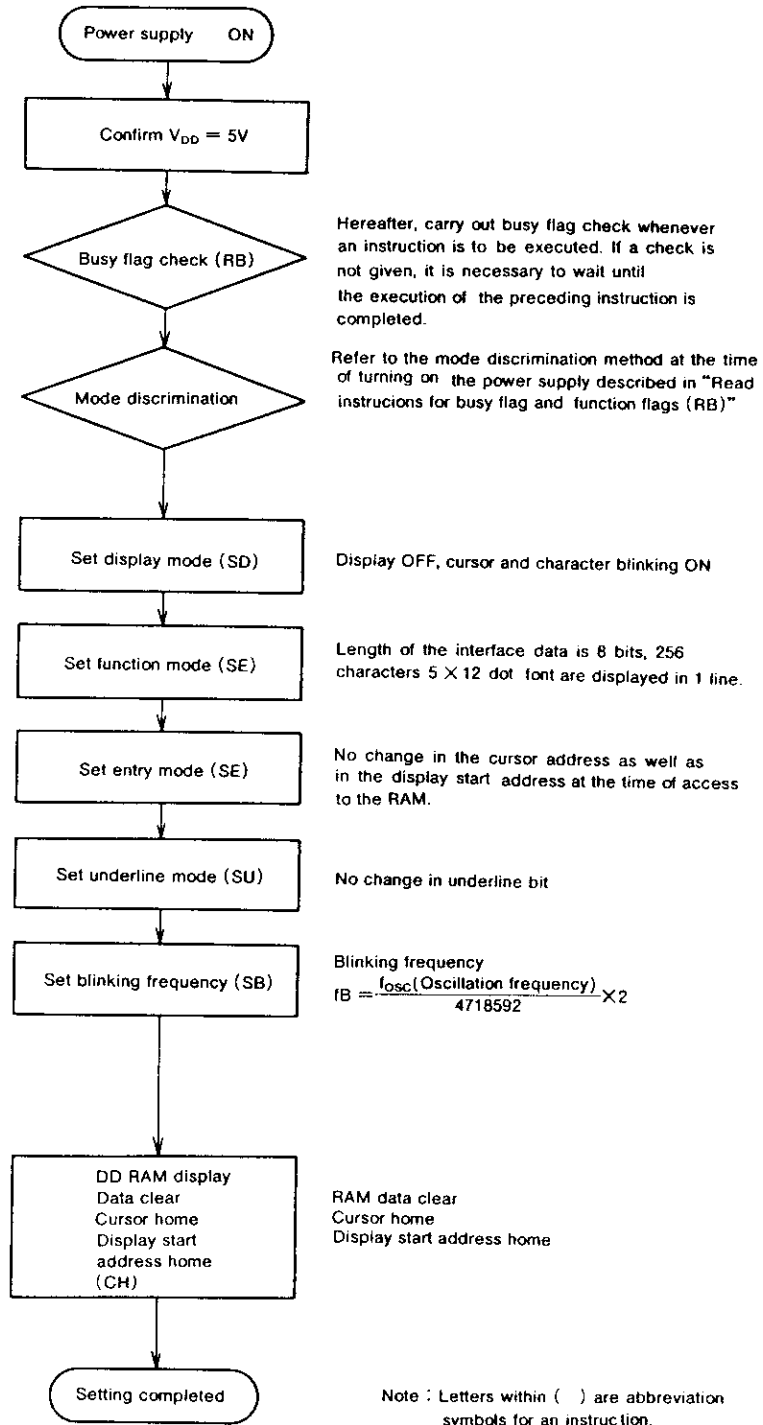


Fig.14 V_{DD} waveform

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

An example of a software initialization method is shown below.

Example of Set Data (for 8-bit mode)										
I/O C1	I/O C2	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
0	0	1	Flag check							
0	0	0	0	0	1	0	0	0	1	1
0	0	0	1	1	1	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1	0	1
0	0	0	0	0	0	0	1	0	1	1
0	0	0	0	0	0	0	0	0	0	1



DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

INSTRUCTION CODE

Instruction Code

Instruction Code											D B	Instruction Function	Execution Time for $f_{osc}=2.58\text{MHz}$	Abbreviation for Instruction									
I/OC	I/OC	R/W																					
1	2		7	6	5	4	3	2	1	0													
1	1	1	AD ₇	AD ₆	AD ₅	AD ₄	AD ₃	AD ₂	AD ₁	AD ₀	Output	Read cursor address of RAM	20 μ s	RC									
		0	AD ₇	AD ₆	AD ₅	AD ₄	AD ₃	AD ₂	AD ₁	AD ₀	Input	Write cursor address of RAM	20 μ s	WC									
		1	AD ₇	AD ₆	AD ₅	AD ₄	AD ₃	AD ₂	AD ₁	AD ₀	Output	Read display start address	20 μ s	RS									
		0	AD ₇	AD ₆	AD ₅	AD ₄	AD ₃	AD ₂	AD ₁	AD ₀	Input	Write display start address	20 μ s	WS									
1	1	1	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Output	Read RAM data	20 μ s	RD									
		0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Input	Write RAM data	20 μ s	WD									
		1	BUSY	4 μ 2	I/O 8/4	FONT 8/12	BUSY	4 μ 2	RAM RA ₁	RAM RA ₀	Output	Read busy flag and other flags	0	RB									
		0	1	1	I/O 8/4	FONT 8/12	DT ₁	DT ₀	RAM RA ₁	RAM RA ₀	Input	Set function mode	20 μ s	SF									
0	0	0	1	1	1	1	1	1	1	1	Input	Set entry mode	20 μ s	SE									
											Input	Set display mode	20 μ s	SD									
											Input	Shift cursor/display-start address	20 μ s	MA									
											Input	Set underline mode	20 μ s	SU									
											Input	Write RAM underline bit	20 μ s	WU									
											Input	Set blinking frequency	20 μ s	SB									
											Input	Cursor home and display start address home	20 μ s	MH									
											Input	Clear cursor of DD RAM display data home, and display start address home	1.25ms	CH									
											Input	No operation	20 μ s	NOP									

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

DESCRIPTION OF INSTRUCTIONS

1 THE READ CURSOR ADDRESS INSTRUCTION (RC)

READ DD/CG RAM CURSOR ADDRESS

This instruction reads the cursor address which designates the RAM address. It reads the 8-bit ($AD_7 \sim AD_0$) cursor address register to the data bus ($DB_7 \sim DB_0$).

The most significant bit (MSB) of the address data is AD_7 and the least significant bit (LSB) is AD_0 .

The cursor address can be used for address designation of writing and reading for both DD RAM and CG RAM.

This instruction enable the value of the current cursor address to be determined.

Instruction code

I/OC	I/OC	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	2									
1	1	1	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0

Input to the LSI

Output from the LSI

2 THE WRITE CURSOR ADDRESS INSTRUCTION (WC)

WRITE DD/CG RAM CURSOR ADDRESS

This instruction writes a cursor address which designates the RAM address. It writes the 8-bit data ($AD_7 \sim AD_0$) on the data bus ($DB_7 \sim DB_0$) to the cursor address register.

The most significant bit (MSB) of the address data is AD_7 and the least significant bit (LSB) is AD_0 .

The cursor address can be used in address designation for writing and reading of both DD RAM and CG RAM.

Instruction code

I/OC	I/OC	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	2									
1	1	0	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0

Input to the LSI

3 THE READ DISPLAY START ADDRESS INSTRUCTION (RS)

READ DISPLAY START ADDRESS

This instruction reads the display start address.

It reads the 8-bit ($AD_7 \sim AD_0$) display start address register to the data bus ($DB_7 \sim DB_0$).

The most significant bit (MSB) of the address data is AD_7 and the least significant bit (LSB) is AD_0 .

The display start address conforms to the RAM address that corresponds to the leftmost digit of the LCD.

This instruction enable the current value of the display start address to be determined.

Instruction code

I/OC	I/OC	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	2									
1	0	1	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0

Input to the LSI

Output from the LSI

4 THE WRITE DISPLAY START ADDRESS INSTRUCTION (WS)

WRITE DISPLAY START ADDRESS

This instruction writes the display start address.

It writes the 8-bit data ($AD_7 \sim AD_0$) on the data bus ($DB_7 \sim DB_0$) to the display start address register.

The most significant bit (MSB) of the address data is AD_7 and the least significant bit (LSB) is AD_0 .

The display start address corresponds to the RAM address that corresponds to the leftmost digit of the LCD. In the 2-line and 4-line display, the display start address agrees with the RAM address that corresponds to the leftmost digit to the first line.

The region of the display start address for various DD RAM regions and numbers of display lines are shown Table.12. Choose the display start address within the range indicated.

Instruction code

I/OC	I/OC	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	2									
1	0	0	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0

Input to the LSI

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

Table 12. Range of display start address

Instruction SF		1-line Display	2-line Display	4-line Display
DT ₁	DT ₁	0	0	1
	D _{T0}	0	1	0
0	0	0~255	0~127	0~63
0	1	0~223	0~111	0~55
1	0	0~191	0~95	0~47
1	1	0~159	0~79	0~39

5 THE READ RAM DATA INSTRUCTION

READ DD/CG RAM DATA

This instruction reads RAM data.

It reads the 8-bit data (D₇~D₀) of the DD RAM or CG RAM designated by the cursor address to the data bus (DB₇~DB₀).

The most significant bit (MSB) of the data is D₇ and the least significant bit (LSB) is D₀.

After the RAM data is read, the cursor address or the display start address is incremented (+1) or decremented (-1) according to the entry mode conditions.

(See the entry mode instruction SE.)

Instruction code

I/OC	I/OC	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
1	2									
0	1	1	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

Input to the LSI

Output from the LSI

6 THE WRITE RAM DATA INSTRUCTION (WD)

WRITE DD/CG RAM DATA

This instruction writes data to the RAM.

It writes the 8-bit data (D₇~D₀) of the data bus (DB₇~DB₀) to the DD RAM address or the CG RAM address which is designated by the cursor address.

The most significant bit (MSB) of the data is D₇ and the least significant bit (LSB) is D₀.

When the system is set to USR=1, the instruction SU sets the underline bit of the cursor address RAM data to (1)₂ when UND S/R=1, and resets to (0)₂ when UND S/R=0. (See the underline mode set instruction SU.)

After writing data to the RAM, the cursor address or the display start address is incremented (+1) or decremented (-1) according to the entry mode conditions. (See the entry mode set instruction SE.)

Instruction code

I/OC	I/OC	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
1	2									
0	1	0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

Input to the LSI

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER
7 THE READ BUSY FLAG AND FUNCTION FLAGS INSTRUCTION (RB)
READ BUSY FLAG & FUNCTION FLAGS

Instruction code

I/OC 1	I/OC 2	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
0	0	1	BUSY	4 μ 2	I/O 8/4	FONT 8/12	BUSY	4 μ 2	RAM	
									RA ₁	RA ₀

Input to the LSI

Output from the LSI

The busy flag and the 4 function mode flags are read to the data bus (DB₇~DB₀) by this instruction. In DB₇ and DB₃ the status of the busy flags (which show whether an instruction other than the instruction RB is in execution) is read.

If BUSY=1, the LSI is executing an instruction.

If BUSY=0, instruction execution is completed.

The busy flags are the flags which show whether the M50530-XXXFP can accept an external instruction. Therefore, when it is desired to issue an external instruction other than the RB to M50530-XXXFP, be sure to read the busy status using instruction RB. If BUSY=1, issue the instruction RB repeatedly until BUSY=0. Issue the next instruction after confirmation that BUSY=0.

In DB₅, DB₄, DB₁, and DB₀, the flag status of the 4 function modes that were set by the function mode set instruction SF and read out.

I/O 8/4 Interface data length flag

FONT 8/12 Font flag

RA₁, RA₀ RAM region flags

In DB₆ and DB₂ (4 μ 2) the flag statuses indicating the current instruction state of the M50530-XXXFP are output to the interfaces with the 8-bit and 4-bit microcomputers.

When 85/ μ c is in the "L" state, the result of execution of the instruction RB is as shown in Table. 13.

It is to be noted that when 85/ μ c is in "H" state, DB₆ and DB₂ always go to "L" state.

Show in Fig. 15, an example of status discrimination by means of the flags is presented.

8 THE SET FUNCTION MODE INSTRUCTION (SF)
SET FUNCTION MODE.

Instruction code

I/OC 1	I/OC 2	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
0	0	0	1	1	I/O 8/4	FONT 8/12	DUTY		RAM	
							DT ₁	DT ₀	RA ₁	RA ₀

Input to the LSI

This instruction sets up the interface width, font, duty, and RAM region.

These prerequisites to the internal data processing are set by the instruction code as follows.

The I/O 8/4 determines the width of the data to be transferred through the external interface.

◦ I/O 8/4 = 1 : The 8 lines of the input/output data bus (DB₇~DB₀) are used for the transfer of 8-bit data. Interfacing with an 8-bit μ c is possible.

◦ I/O 8/4 = 0 : 8-bit data is transferred in 2 portions (the upper 4 bits and the lower 4 bits), by using the high nibble (DB₇~DB₄) of the 8 input/output data bus (DB₇~DB₀).

Interfacing with a 4-bit μ c is possible.

The FONT 8/12 determines the dot matrix composition for one character font.

◦ FONT 8/12 = 1 : The font for 1 digit is composed of 5 $\times$ 8 dots. Of these, 5 $\times$ 7 dots are for the character font, and the 5 $\times$ 1 dots in the bottom row are for the cursor.

◦ FONT 8/12 = 0 : The font for 1 digit is composed of 5 $\times$ 12 dots. Of these 5 $\times$ 11 dots are for the character font, and the 5 $\times$ 1 dots in the bottom row for the cursor.

The DUTY (DT₁ and DT₀) sets the duty and the line number of the display. The RAM (RA₁ and RA₀) sets the DD region and the CG region.

This is shown in Table. 14.

Table 13. Result of executed instruction RB.

		Data BUS								
		DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀	
		BUSY	4 μ 2	I/O 8/4	FONT 8/12	BUSY	4 μ 2	RA ₁	RA ₀	
8-bit mode		BUSY	L	H	8/12	BUSY	"L"	RA ₁	RA ₀	Result of execution in 8-bit operation mode
4-bit mode	First half data	BUSY	"L"	"L"	8/12					Result of execution in first 4-bit operation mode
	Second half data	BUSY	"H"	RA ₁	RA ₀					Result of execution in second 4-bit operation mode

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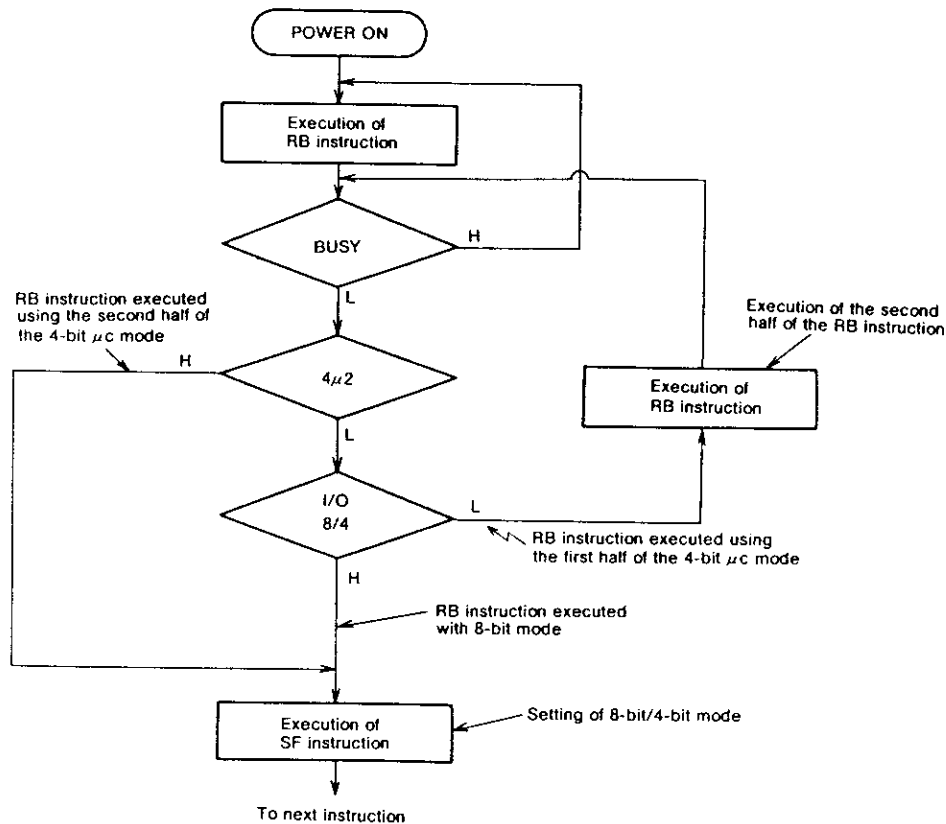


Fig.15 Example of status discrimination

Mode discrimination method at the time of turning on the power supply (when the power on clear is inoperative)

Table 14. Region of RAM

Instruction SF		RAM (9 bits for 1 Word)						
		DD RAM			CG RAM			
		1-line Display	2-line Display	4-line Display				
FONT	1	Duty 1/8	Duty 1/16	Duty 1/32	CG character number FONT 8/12			
	8/12	Duty 1/12	Duty 1/24	Duty 1/48				
	DT ₁	0	0	1				
	DT ₀	0	1	0				
RA ₁	RA ₀							
0	0	1 lineX256 words	2 lineX128 words	4 lineX 64 words	0word	0character	0character	
0	1	1 lineX224 words	2 lineX112 words	4 lineX 56 words	32words	4character	2character	
1	0	1 lineX192 words	2 lineX 96 words	4 lineX 48 words	64words	8character	4character	
1	1	1 lineX160 words	2 lineX 80 words	4 lineX 40 words	96words	12character	6character	

Please refer to item DD/CG RAM Regarding the RAM addresses.

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

9 THE SET DISPLAY MODE INSTRUCTION (SE)

SET ENTRY MODE

This instruction determines whether the cursor address or the display start address is incremented (+1) or decremented (−1) after writing a data in the RAM with the instruction WD, or after reading a data from the RAM with the instruction RD.

The conditions for the cursor address and the display start address can be set independently of each other. The setting conditions are shown in Table 15, 16.

Instruction code

I/OC 1	I/OC 2	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
0	0	0	0	1	CSR D/I	CSR CONDITION W R		DSP D/I	DSP CONDITION W R	

Input to the LSI

Table 15. Cursor Address setting Conditions

CSR D/I	CSR CONDITION		Cursor Address
	W	R	
X	0	0	No change in the cursor address occurs due to the instruction WD or RD.
1	0	1	The cursor address is decremented after reading the data with the instruction RD.
0	0	1	The cursor address is incremented after reading the data with the instruction RD.
1	1	0	The cursor address is decremented after writing data using the instruction WD.
0	1	0	The cursor address is incremented after writing data using the instruction WD.
1	1	1	The cursor address is decremented after execution of the instruction WD or RD.
0	1	1	The cursor address is incremented after execution of the instruction WD or RD.

Table 16. Display Start Address setting Conditions

DSP D/I	DSP CONDITION		Display Start Address
	W	R	
X	0	0	No change in the display start address occurs due to the instruction WD or RD.
1	0	1	The display start address is decremented after reading the data with the instruction RD.
0	0	1	The display start address is incremented after reading the data with the instruction RD.
1	1	0	The display start address is decremented after writing data with the instruction WD.
0	1	0	The display start address is incremented after writing data with the instruction WD.
1	1	1	The display start address is decremented after execution of the instruction WD or RD.
0	1	1	The display start address is incremented after execution of the instruction WD or RD.

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10 THE SET DISPLAY MODE
INSTRUCTION (SD)
SET DISPLAY MODE

Instruction code

I/OC 1	I/OC 2	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
0	0	0	0	0	1	DSP ON/OFF	CSR ON/OFF	UND ON/OFF	CSR BLINK	CHR BLINK

Input to the LSI

This instruction sets the display modes.

The following display modes can be set by this instruction code.

- DSP ON/OFF=1 : This turns on all displays.
DSP ON/OFF=0 : This turns off all displays.
- CSR ON/OFF=1 : This turns on the cursor display.
CSR ON/OFF=0 : This turns off the cursor display.
- UND ON/OFF=1 : This turns on the underline display.
UND ON/OFF=0 : This turns off the underline display.
- CSR BLINK=1 : This causes the cursor display to blink.
CSR BLINK = 0 : This displays the
cursor display

without blinking.

- CHR BLINK=1 : This causes the character display of the
cursor position to blink.
CHR BLINK=0 : This displays the character display with-
out blinking.

The blink displays are presented as shown Fig. 16 depend-
ing upon the position of the cursor.

11 THE SHIFT CURSOR/DISPLAY-START
ADDRESS INSTRUCTION (MA)
MOVE CURSOR/DISPLAY ADDRESS

Instruction code

I/OC 1	I/OC 2	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
0	0	0	0	0	0	1	CSR D/I	DSP D/I	DSP D/I	DSP D/I

Input to the LSI

This instruction increments (+1) or decrements (−1) the
cursor address or the display start address.

The cursor address and the display start address can be
incremented or decremented independently of each other.

The results of the execution of the instruction code are as
shown Table 17, 18.

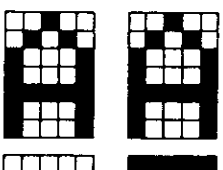
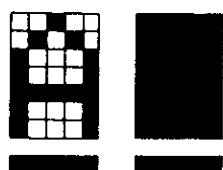
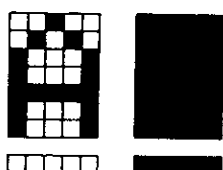
CSR ON/OFF	1	1	1
CSR BLINK	1	0	1
CHR BLINK	0	1	1
Examples are for a 5X8 dot matrix			
	Displayed alternately	Displayed alternately	Displayed alternately

Fig.16 Example of blinking

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Table 17. Shift of cursor address

CSR	CSR D/I	Cursor Address
0	X	No change occurs in the cursor address.
1	1	This decrements the cursor address. The cursor appears to be shifted to the left.
1	0	This increments the cursor address. The cursor appears to be shifted to the right.

Table 18. Shift of display start address

DSP	DSP D/I	Display Start Address
0	X	No change occurs in the display start address.
1	0	The display start address is decremented. The display as a whole appears to be shifted to the right.
1	0	The display start address is incremented. The display as a whole appears to be shifted to the left.

12 THE SET UNDERLINE MODE INSTRUCTION (SU) *

SET UNDERLINE MODE

Instruction code

I/OC 1	I/OC 2	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
0	0	0	0	0	0	0	1	1	USR ON/OFF	UND S/R

Input to the LSI

This instruction determines whether or not to set or reset the underline bit at the time of writing an 8-bit data in the RAM by means of the instruction WD.

The instruction code can set Table 19 conditions:

When display data for which the underline bit is set is displayed in the underline display mode, a (5×1) dot underline will be displayed at the bottom row position of the dot matrix (position where the 5×1 dot cursor line is displayed), in addition to the character display.

Since every word in the RAM carries an underline bit, one can set the underline display for every character displayed.

* Note: The "UND" of 1g, 1/2 and 1/4 is not in SD bit.

Table 19. Set underline mode.

USR ON/OFF	UND S/R	Underline Bit Set/Reset Mode
1	1	One can set the underline bit by means of the instruction WD following the execution of this instruction SU.
1	0	One can reset the underline bit by means of the instruction WD following the execution of this instruction SU.
0	X	The set/reset mode is canceled so that the underline bit will neither be set nor reset by the instruction WD.

13 THE WRITE UNDERLINE BIT INSTRUCTION (WU) WRITE UNDERLINE BIT

Instruction code

I/OC 1	I/OC 2	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
0	0	0	0	0	0	0	1	0	UND S/R	CSR I

Input to the LSI

This instruction sets or resets the underline bit in the 9-bit data of the cursor address of the RAM. It can also increment the cursor address after setting or resetting. This instruction performs Table 20 operations.

When display data for which the underline bit is set is displayed in the underline display mode, a 5×1 dot underline at the position of the bottom row of the dot matrix (position where the cursor line with 5×1 dot is displayed) will be displayed, in addition to the display of characters.

Since every word of the RAM carries an underline bit, the underline display can be set for every word in the display.

Table 20. Set underline and cursor address

UND S/R	CSR I	Underline Bit/Cursor Address
1	1	After setting the underline bit, the cursor address is incremented.
1	0	This sets the underline bit. No change occurs in the cursor address.
0	1	After resetting the underline bit, the cursor address is incremented.
0	0	This resets the underline bit. No change occurs in the cursor address.

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14 THE SET BLINK FREQUENCY INSTRUCTION (SB)

SET BLINK FREQUENCY

This instruction sets the blinking frequency for the cursor line or a character situated at the position of the cursor. The blinking frequencies are assigned by the instruction code as Table 21.

Table 21. Blinking frequency

B ₁	B ₀	Blinking Frequency
0	0	$f_b = f_{osc}/4718592$
0	1	$f_b = (f_{osc}/4718592) \times 2$
1	0	$f_b = (f_{osc}/4718592) \times 4$
1	1	$f_b = (f_{osc}/4718592) \times 8$

Here, f_{osc} is the oscillation frequency of the oscillator.

Instruction code

I/OC 1	I/OC 2	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
0	0	0	0	0	0	0	0	1	B ₁	B ₀

Input to the LSI

15 THE DISPLAY/CURSOR ADDRESS HOME INSTRUCTION (MH)

MOVE DISPLAY/CURSOR ADDRESS HOME

This instruction writes (00)₁₆ in the display start address register and the cursor address register. By this, both the display address and the cursor address are set to the home address.

Instruction code

I/OC 1	I/OC 2	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
0	0	0	0	0	0	0	0	0	1	1

Input to the LSI

16 THE CLEAR DISPLAY/ADDRESS HOME INSTRUCTION (CH)

CLEAR DISPLAY, MOVE DISPLAY/CURSOR ADDRESS HOME

This instruction converts all of the 8-bit display data of the RAM display data region to the space code, and all of the underline bits to (0)₂ (nondisplaying.)

In addition, it writes (00)₁₆ to the display start address register and the cursor address register. By this, both the display start address and the cursor address are set to the home address.

Instruction code

I/OC 1	I/OC 2	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
0	0	0	0	0	0	0	0	0	0	1

Input to the LSI

17 THE NO OPERATION INSTRUCTION (NOP)

NO OPERATION

This is the instruction for doing nothing. No change occurs from this instruction.

Instruction code

I/OC 1	I/OC 2	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
0	0	0	0	0	0	0	0	0	0	0

Input to the LSI

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

INTERFACES WITH μc AND μp

M50530-XXXFP can interface directly with 4-bit μc , 8-bit μc and 8085 μp .

1 The interface with 8-bit μc

The 8-bit μc and M50530-XXXFP are connected as Fig. 17: The output ports of the 8-bit μc are connected to the EX, I/O C1, I/O C2, and R/W terminals of M50530-XXXFP. The input/output port of the 8-bit μc , is connected to the data bus terminal of M50530-XXXFP.

By giving an input/output instruction to the 8-bit μc , via the ports, to the I/O C1, I/O C2, R/W, and $DB_7 \sim DB_0$ terminals, M50530-XXXFP will execute the instruction.

If one designates instructions other than RB (read busy flag and function flags) by IR (NOT RB), then M50530-XXXFP assigns $(1)_2$ to the busy flag to indicate that it is executing an instruction, when it is executing autoclear at the time of closing the power supply or it is executing an instruction IR (NOT RB). When the busy flag is set $(1)_2$, even if a subsequent instruction IR (NOT RB) is given, M50530-XXXFP will not execute it. Accordingly, in giving an instruction to M50530-XXXFP, it is necessary to examine, using the read busy flag instruction RB, whether the busy flag is $(1)_2$ or $(0)_2$. If it is $(0)_2$, an instruction IR (NOT RB) given next to M50530-XXXFP will be executed.

Fig. 18 is an example of instructions exchange between the 8-bit μc and the M50530-XXXFP timing sequence.

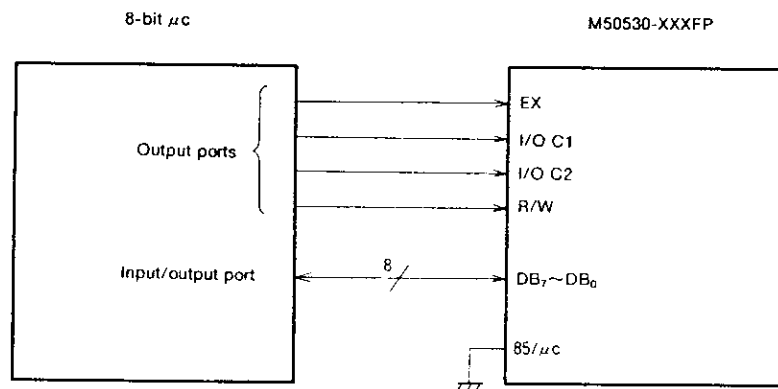


Fig.17 Interface with 8-bit μc .

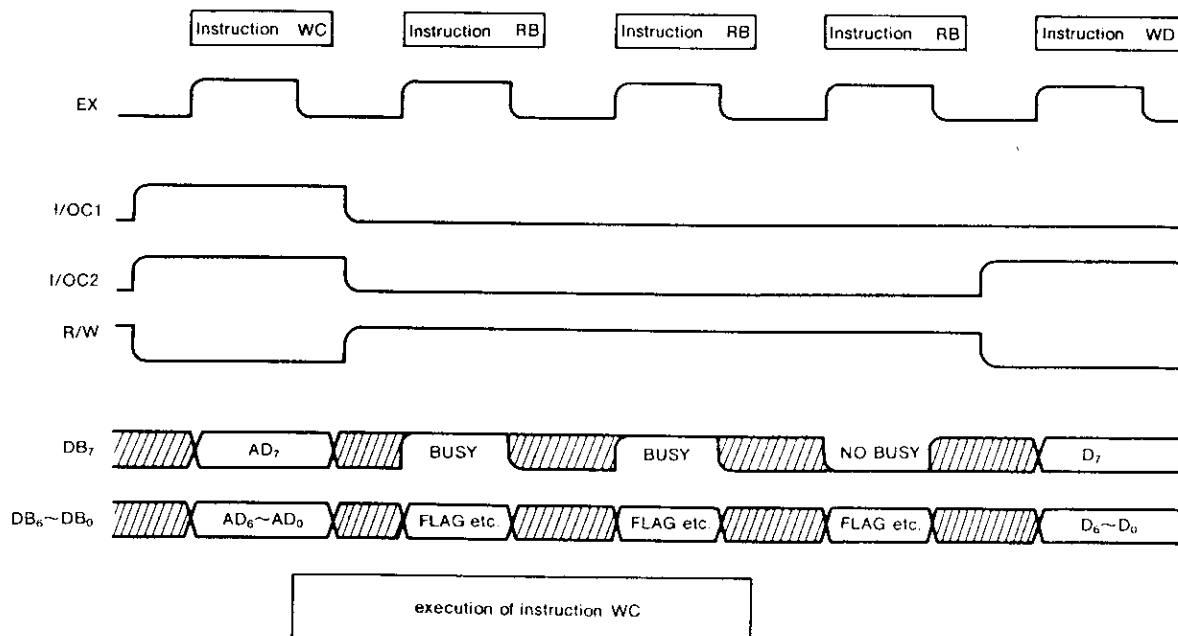


Fig.18 Interface timing with 8-bit μc

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

2 The interface with 4-bit μ c

The 4-bit μ c and M50530-XXXXFP are connected as shown Fig. 19.

The output ports of the 4-bit μ c are connected to the EX, I/OC1, I/OC2, and R/W terminals of M50530-XXXXFP, and the input/output port of the 4-bit μ c is connected to the upper 4-bit terminals of M50530-XXXXFP data bus (DB₇ ~ DB₄). The lower 4-bit terminals (DB₃ ~ DB₀) of the data bus are left disconnected, and will not be used in this case.

To simplify the explanation, the data bus instruction code DB₇ ~ DB₀ for the 8-bit is renamed in the 4-bit μ c mode. The upper 4-bit instruction code is defined as UB₇ ~ UB₄ and the lower 4-bit instruction code will be defined as LB₃ ~ LB₀.

Data Bus Instruction Code	
8-bit mode	4-bit mode
DB ₇ ~ DB ₄	UB ₇ ~ UB ₄
DB ₃ ~ DB ₀	LB ₃ ~ LB ₀

In the case of the 8-bit μ c, the EX signal is applied one time to execute an instruction. However, in the case of the 4-bit μ c mode, the data bus is used twice to execute one instruction, as such it is absolutely necessary to start execution by applying the EX signal twice. Therefore, identical instruction codes are given to the I/OC1, I/OC2, and R/W terminals for both the first and second times. UB₇ ~ UB₄ are given to the data bus terminals DB₇ ~ DB₄ the first time and LB₃ ~ LB₀ the second time. If the instructions other than the read busy flag and function flags instruction RB are called IR (NOT RB), during execution of autoclear at the time of closing of the power supply and during execution of an instruction IR (NOT RB), M50530-XXXXFP shows (1)₂ for the busy flag, indicating that it is in execution of an instruction. When the busy flag is set (1)₂, even when the next instruction IR (NOT RB) is given to M50530-XXXXFP, the instruction will not be executed.

Therefore, busy flag status, (1)₂ or (0)₂, must be examined, by means of the read busy flag instruction RB before initiating an instruction. If the flag is (0)₂, the next instruction IR (NOT RB) given to M50530-XXXXFP will be executed.

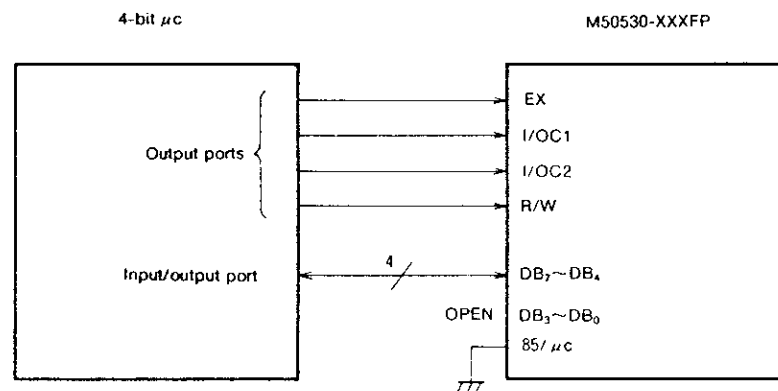


Fig.19 Interface with 4-bit μ c.

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

In the case of the 4-bit μ c, it is necessary to apply EX signal twice times for the execution of an instruction. When the power supply is turned on, it is in the 8-bit μ c mode. If 4-bit μ c mode is desired, then instruction SF is given after confirming the completion of the autoclear operation. This is done with the use of the read busy flag and

function flags instruction RB subsequent to the closing of the power supply (at this time still in the 8-bit mode). The instruction SF at this time is 4-bit μ c mode instruction, and it is necessary to hold for two EX signals. Fig. 20 is a timing sequence diagram example of an instruction exchange between the 4-bit μ c and the M50530-XXXFP.

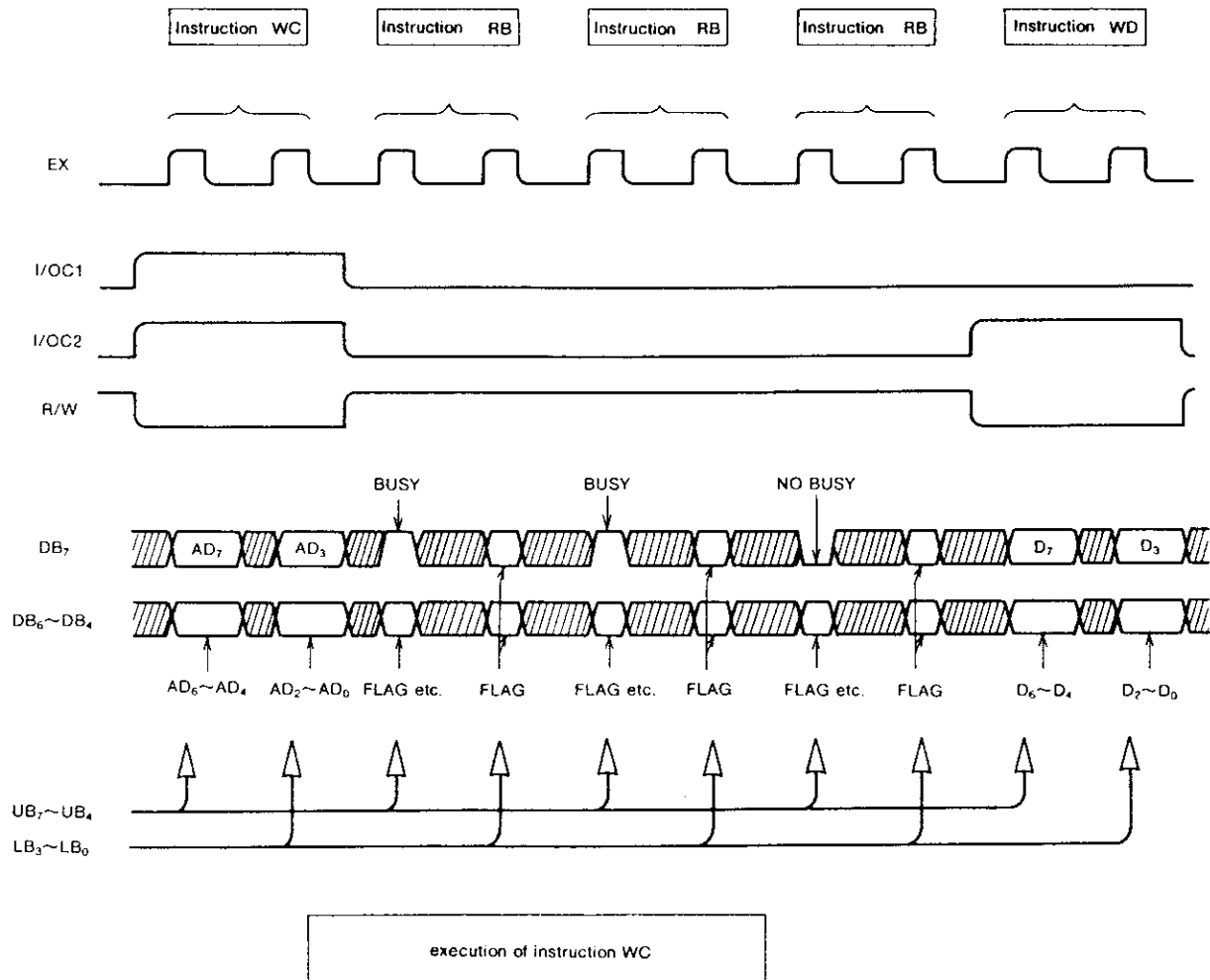


Fig.20 Interface timing with 4-bit μ c.

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

3 The interface with 8085 μ p (μ p mode)

The 8-bit μ p 8085 and M50530-XXXFP are connected as shown in Fig. 21.

In this mode the signal terminals ALE, $\overline{RD}$, $\overline{WR}$, and $\overline{IOM}$ unique to the 8085 μ p are connected to the EX, R/W, I/OC1, and I/OC2 terminals of the M50530-XXXFP. The address data bus $AD_7 \sim AD_0$ of the 8085 μ p is connected to the data bus $DB_7 \sim DB_0$ of M50530-XXXFP.

The instruction codes I/OC1, I/OC2, and R/W from the μ c mode are sent in this mode on the address data bus $AD_7 \sim AD_0$.

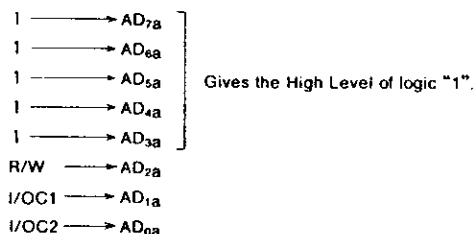
The terminals for the signals R/W, I/OC1, and I/OC2 of the M50530-XXXFP become independent of the instruction codes, and come to be used exclusively for $\overline{RD}$, $\overline{WD}$, and $\overline{IOM}$ of 8085.

To give an instruction to M50530-XXXFP from the 8085, the 8085 input and output instructions IN and OUT are used. When the $\overline{IOM}$ signal is "H", the 8085 sends two kinds of data on the 8-bit address data bus $AD_7 \sim AD_0$. Of these, if the data sent first is designated $AD_{7a} \sim AD_{0a}$ and the next data sent is designated $AD_{7b} \sim AD_{0b}$, then

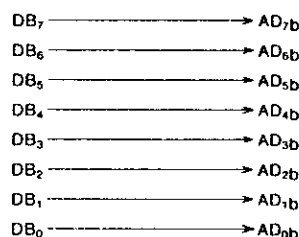
$AD_{7a} \sim AD_{0a}$ is I/O port address and

$AD_{7b} \sim AD_{0b}$ is read or write data

By using the address data bus in the above for the 8085 input and output instructions IN and OUT, M50530-XXXFP is controlled as shown below.



Next, of the instruction codes, $DB_7 \sim DB_0$ are placed on $AD_{7b} \sim AD_{0b}$ as shown below.



In the above, the address (chip select) when M50530-XXXFP is seen as an I/O port is given by

$(AD_{7a}, AD_{6a}, AD_{5a}, AD_{4a}, AD_{3a}, AD_{2a}, AD_{1a}, AD_{0a}) = (1111xxx)_2$

where the symbol x stands for 1 or 0.

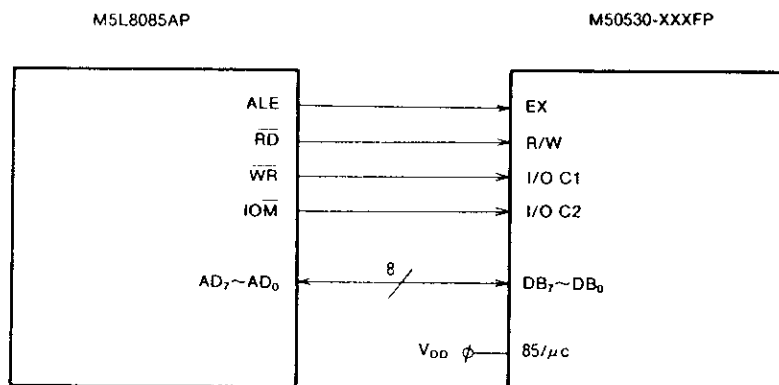


Fig.21 Interface with 8085 μ p.

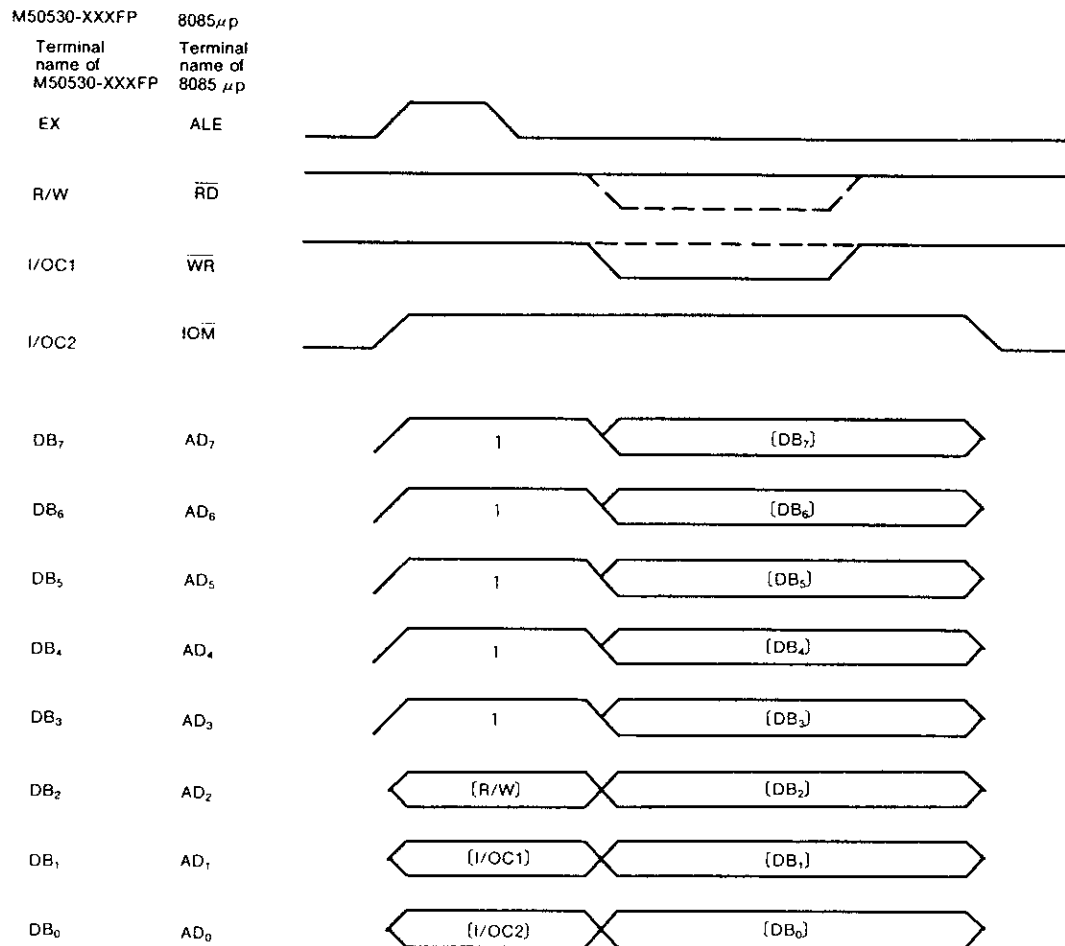
DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

A timing sequence diagram example of the instruction exchange between the 8085 μ p and the M50530-XXXFP is shown in Fig. 22.

When many instructions are executed, the $\overline{\text{IOM}}$ signal of the μ p mode (8085 μ p) corresponds to the EX signal of the μ c mode (8-bit μ c mode).

In all other cases, the instruction sequence is similar for the μ p mode and the μ c mode.

However, the data width of DB in the μ p mode has 8 bits, and it is not possible to set the I/O interface to the 4-bit mode by means of the instruction SF.



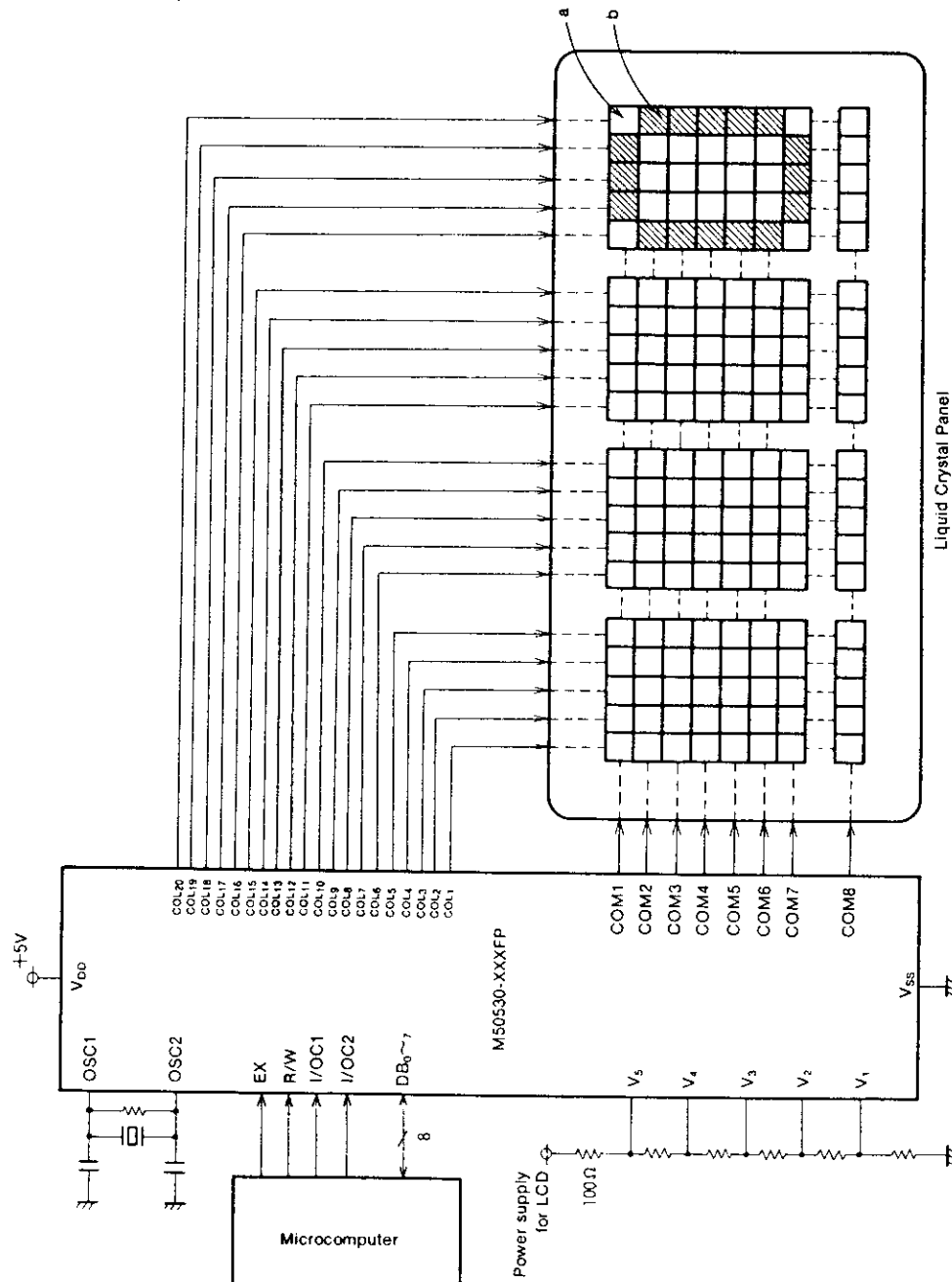
In the above, [] shows an instruction code.

Fig.22 Interface timing with 8085 μ p

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

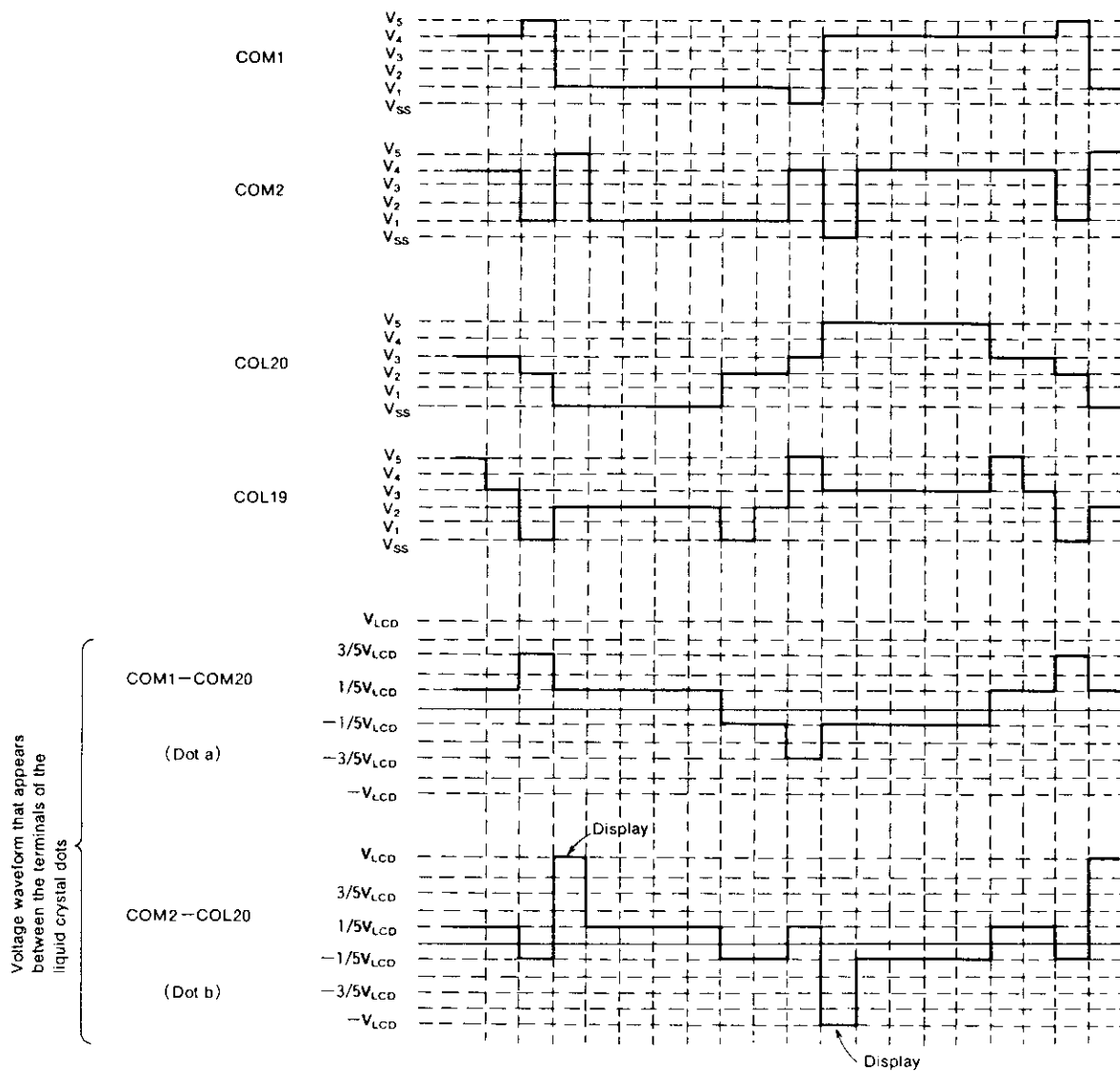
AN EXAMPLE OF APPLICATION CIRCUIT AND WAVEFORMS FOR LIQUID CRYSTAL DRIVING

- 1 A circuit example (Display of 4 characters with 5×8 dots)



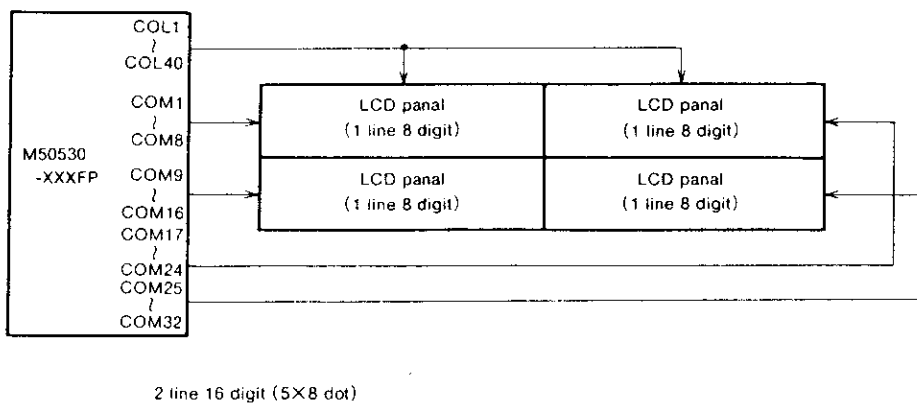
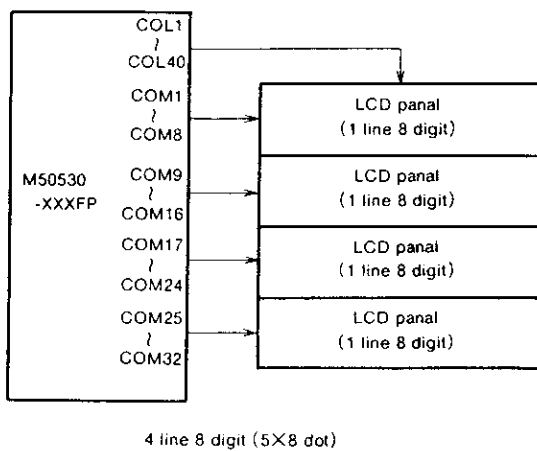
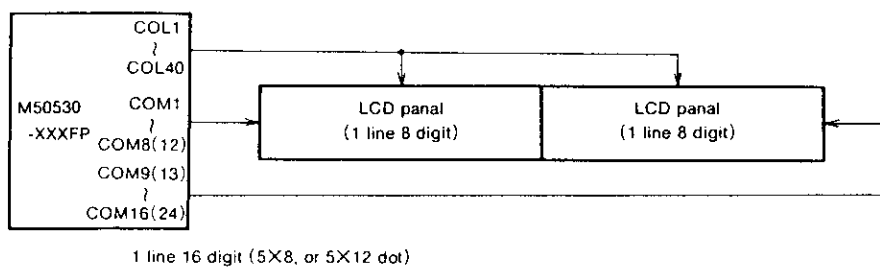
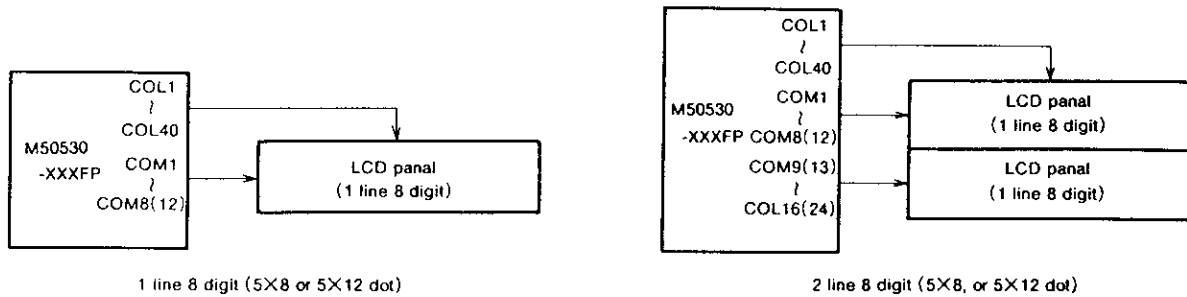
DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

2 Waveforms for liquid crystal driving



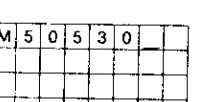
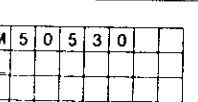
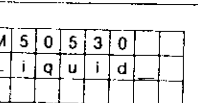
DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

M50530-XXXFP one chip system example

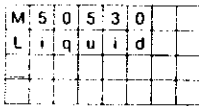
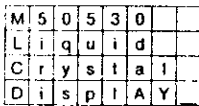
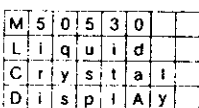
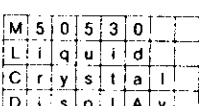
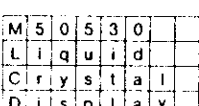


DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

8-bit action, 8 characters × 4 lines display example

No.	Abbreviation	Instruction												Display	Action
		I/O	I/O	R/W	D B										
		C1	C2		7	6	5	4	3	2	1	0			
1	—	Power ON													Initialized by internal reset circuit. Nothing displayed.
2	SF	Set function mode													8-bit action, 4 lines displayed. Font is 5X8 dot
		0	0	0	1	1	1	1	1	0	0	0			
3	SE	Set entry mode													Mode is set to increase cursor address after writing data by instruction WD.
		0	0	0	0	1	0	1	0	0	0	0			
4	SD	Set display mode													Cursor is displayed.
		0	0	0	0	0	1	1	1	0	0	0			
5	WD	Write data to RAM													"M" is displayed, and cursor shifts right.
		0	1	0	0	1	0	0	1	1	0	1			
6	WD	Write data to RAM													"50530" is displayed.
7															
8															
9															
10		0	1	0	X	X	X	X	X	X	X	X			
11	WC	Write cursor address													Cursor moves to 2nd line 1st digit.
		1	1	0	0	1	0	0	0	0	0	0			
12	WD	Write data to RAM													"Liquid" is displayed.
13															
14															
15															
16		0	1	0	X	X	X	X	X	X	X	X			
17															

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

No.	Abbreviation	Instruction										Display	Action	
		I/O C1	I/O C2	R/W	D					B				
					7	6	5	4	3	2	1	0		
18	WC	Write cursor address											Cursor move to 3rd line 1st digit	
		1	1	0	1	0	0	0	0	0	0			0
19	WD												"Crystal" is displayed. Cursor moves to 4th line, 1st digit and "Display" is displayed.	
33	WC													
33	WD													
34	MA	Shift cursor and display start address											Cursor address is decreased. Namely Cursor shifts left. Display start address don't change.	
		0	0	0	0	0	0	1	1	1	0			0
35	MA	Shift cursor and display start address											Cursor address is decreased. Namely Cursor shifts left. Display start address don't change.	
		0	0	0	0	0	0	1	1	1	0			0
36	WD	Write data to RAM											"a" is displayed.	
		0	1	0	0	1	1	0	0	0	0			1
37	MA	Shift cursor and display start address											Only display start address is decreased. Display shifts left.	
		0	0	0	0	0	0	1	0	0	1			0
38	CH	Clear DD RAM data and address home of display start address											Display is cleared, and cursor moves to 1st line 1st digit.	
		0	0	0	0	0	0	0	0	0	0			1

Note) Please enter instructions, after checking busy flag with instruction RB.
If busy flag is set, it is necessary to wait for the execution of the previous instruction before entering new instruction.

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

AN EXTENSION OF THE SYSTEM

The LCD system of the M50530-XXXFP can be expanded by connecting to it an external liquid crystal driver IC M50521FP or M50524FP.

1 AN EXTENSION OF THE COLUMN DRIVER

The M50521FP uses the M50524FP as the column driver. For this case, the SCL, CLD, CS, DST, and FRM terminals of the M50530-XXXFP are connected to the SCL, DI, CSI, DST, and FRM terminals of the driver IC, respectively. A

maximum display of 256 digits (1 line) is possible.

2 AN EXTENSION OF THE COMMON DRIVER

The M50521FP also uses the M50524FP as the common driver. For this case, the CMD, DST, and FRM terminals of the M50530-XXXFP are connected to the CSI, DST, and FRM terminals of the driver IC, respectively. A maximum display of 4 lines (for duty of 1/48) of 5×12 dot characters is possible.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	Logic circuit	-0.3~+7.0	V
$V_1 \sim V_5^*$		LCD driving circuit	-0.3~+15	V
V_i	Input voltage		$V_{SS} - 0.3 \leq V_i \leq V_{DD} + 0.3$	V
T_{opr}	Operating ambient temperature		-20~+70	°C
T_{stg}	Storage temperature		-40~+125	°C
P_d	Maximum power dissipation		300	mW

*In the above, it is assumed that $V_5 > V_4 \geq V_3 \geq V_2 \geq V_1$.

RECOMMENDED OPERATING CONDITIONS ($T_a = -20$ to $+70^\circ\text{C}$)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{DD}	Supply voltage for logic circuit	4.5	5.0	5.5	V
V_5^*	Supply voltage for LCD driving circuit	3		14	V
V_{iL}	"L" input voltage	V_{SS}	V_{SS}	$0.3 \times V_{DD}$	V
V_{iH}	"H" input voltage	$0.7 \times V_{DD}$	V_{DD}	V_{DD}	V
f_{osc}	Clock oscillation frequency	2	2.5	3	MHz

*Connect to V_5 a resistor not less than 47Ω ($\pm 10\%$) in series with the power supply.

ELECTRICAL CHARACTERISTICS (unless otherwise noted, for $V_{DD}=5\text{V}$ at $T_a=25^\circ\text{C}$)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
I_{DD}	Supply current for logic	$f_{osc}=2.5\text{MHz}$			10	mA
I_{V5}	Supply current for LCD	No-load LCD output $V_5=14\text{V}$			100	μA
V_{OL}	"L" output voltage (1)	$I_{OL}=2\text{mA}$			0.4	V
V_{OH}	"H" output voltage (1)	$I_{OH}=-2\text{mA}$	3.5			V
I_i	Input leak current (2)	$V_i=0 \sim V_{CC}$	-10		10	μA
V_{OZ}	OFF-state output current (3)	$V_O=0 \sim V_{CC}$	-10		10	μA
R_{ON}	LCD output ON resistance (4)	$V_5=14\text{V}$			500	Ω
		$V_5=5\text{V}$			2	k Ω

- (1) Applicable to the output terminals: DST, SCL, FRM, CS, CMD, and CLD.
 (2) Applicable to the inputs of $85/\mu\text{C}$: I/OC1, I/OC2, R/W, EX, and OSC1.
 (3) Applicable to the output terminals: DB₇ to DB₀.
 (4) Applicable to each LCD output of COL1 to COL40 and COM1 to COM32.

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

TIMING CHARACTERISTICS UNDER THE 8-BIT μ c CONTROL

(unless otherwise noted, for $V_{DD}=5V$ at $T_a=25^\circ C$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(EX)}$	EX signal pulse width		200			ns
t_{SU}	Control data setup time		200			ns
t_H	Control data hold time		100			ns
$t_{d(EX-D)}$	Data output delay time	$C_L=15pF$			300	ns
$t_{V(EX-D)}$	Data effective time	$C_L=15pF$	300			ns
$t_{SU(D-EX)}$	Data setup time		200			ns
$t_{H(EX-D)}$	Data hold time		100			ns

TIMING CHARACTERISTICS UNDER THE 4-BIT μ c CONTROL

(unless otherwise noted, for $V_{DD}=5V$ at $T_a=25^\circ C$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(EX)}$	EX signal pulse width		200			ns
$t_{C(EX)}$	EX signal interval		800			ns
t_{SU}	Control data setup time		200			ns
t_H	Control data hold time		100			ns
$t_{d(EX-D)}$	Data output delay time	$C_L=15pF$			300	ns
$t_{V(EX-D)}$	Data effective time	$C_L=15pF$	300			ns
$t_{SU(D-EX)}$	Data setup time		200			ns
$t_{H(EX-D)}$	Data hold time		100			ns

TIMING CHARACTERISTICS UNDER THE 8085 μ p CONTROL

(unless otherwise noted, for $V_{DD}=5V$ at $T_a=25^\circ C$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(EX)}$	EX signal pulse width		200			ns
t_{SU}	Control data setup time		200			ns
t_H	Control data hold time		100			ns
$t_{d(D)}$	Data delay time	$C_L=15pF$			300	ns
$t_{V(D)}$	Data effective time	$C_L=15pF$	300			ns
$t_{SU(D)}$	Data setup time		200			ns
$t_{H(D)}$	Data hold time		100			ns

TIMING CHARACTERISTICS FOR EXTENDED SIGNALS

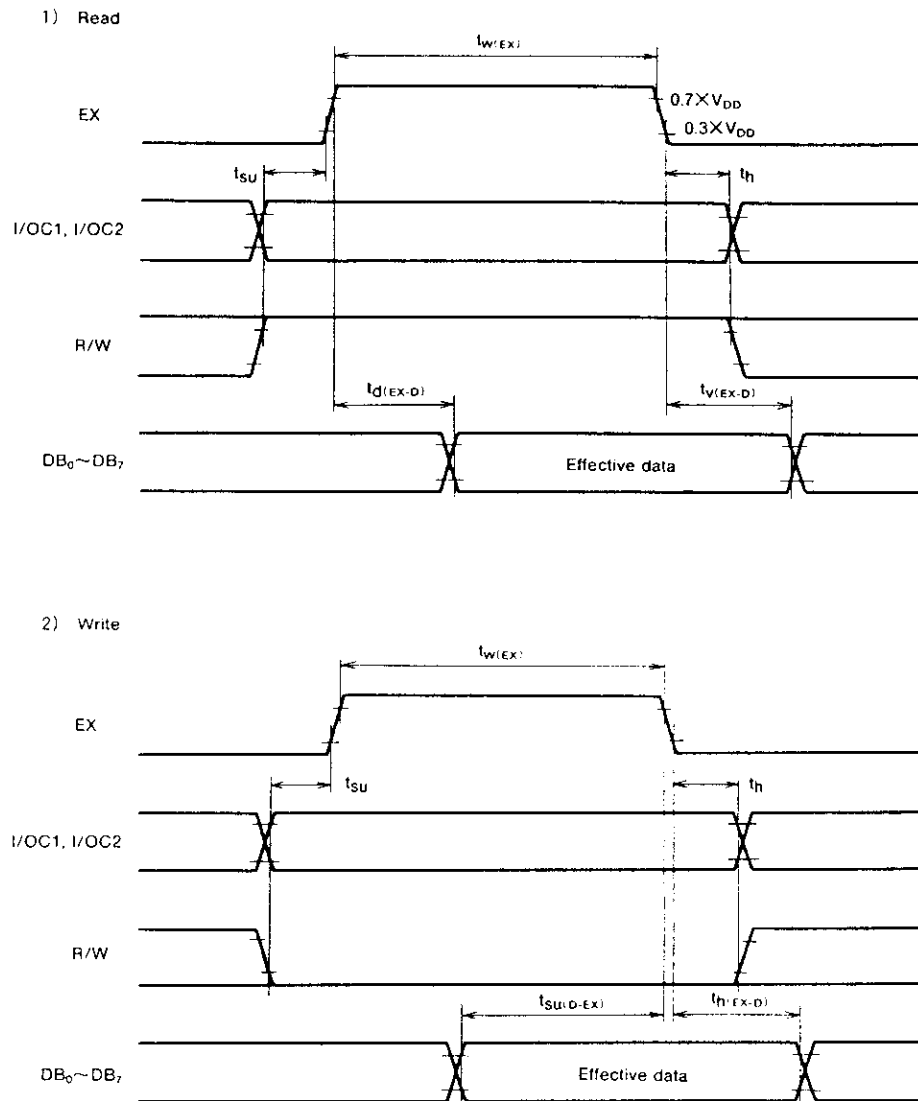
(unless otherwise noted, for $V_{DD}=5V$ and $f_{osc}=3MHz$ at $T_a=25^\circ C$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{WH(SCL)}$	Shift clock "H" pulse width		300			ns
$t_{WL(SCL)}$	Shift clock "L" pulse width		300			ns
$t_{W(CS)}$	Chip select pulse width		300			ns
$t_{H(SCL-CS)}$	Chip select hold time		300			ns
$t_{H(CS-SCL)}$	Shift clock hold time		300			ns
$t_{SU(D)}$	Column data setup time		200			ns
$t_{H(D)}$	Column data hold time		300			ns
$t_{W(DST)}$	Data set pulse time		450			ns
$t_{H(SCL-DST)}$	Data set hold time		600			ns
$t_{W(CMD)}$	Common data pulse width		1950			ns
$t_{SU(CMD-DST)}$	Data setup time		200			ns
$t_{d(DST-FRM)}$	Frame delay time				300	ns

Note : All values refer to the case of load capacity of $C_L=15pF$.

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

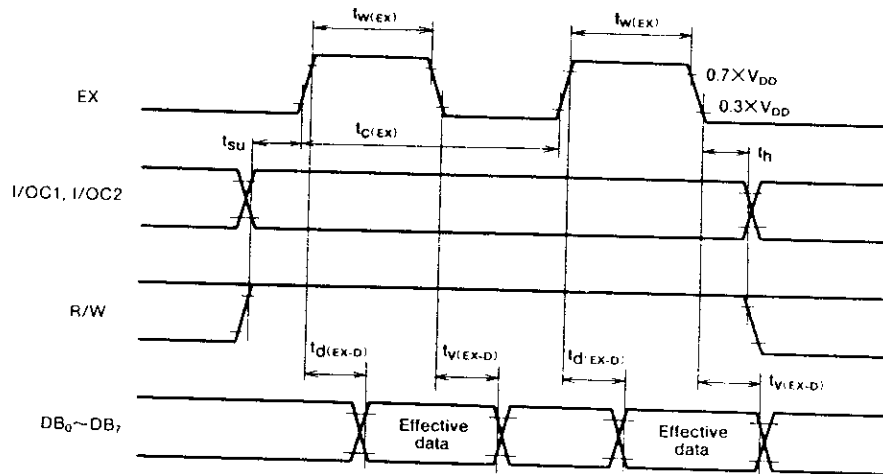
Timing Wave forms under 8-bit μ c Control



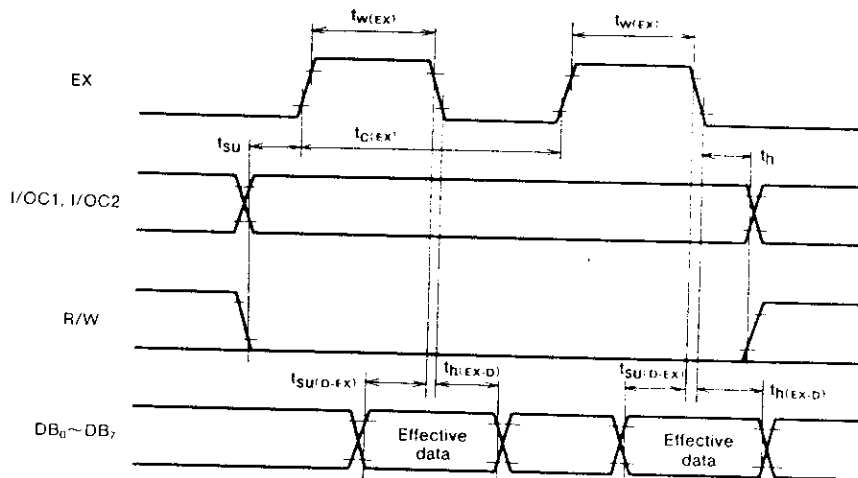
DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

Timing Wave forms under 4-bit μ c Control

1) Read



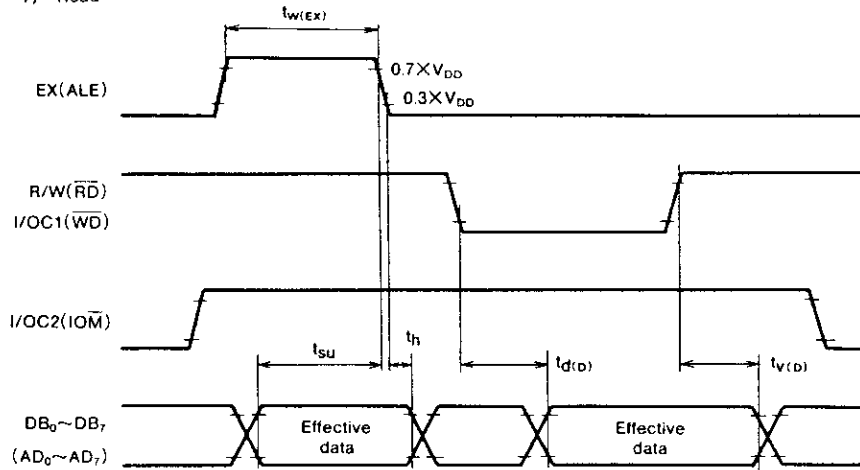
2) Write



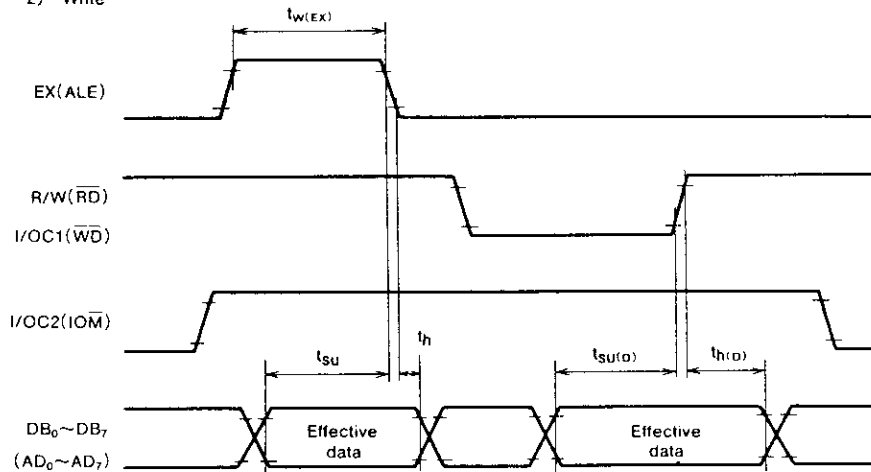
DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

Timing Wave forms under 8085 μ p Control

1) Read

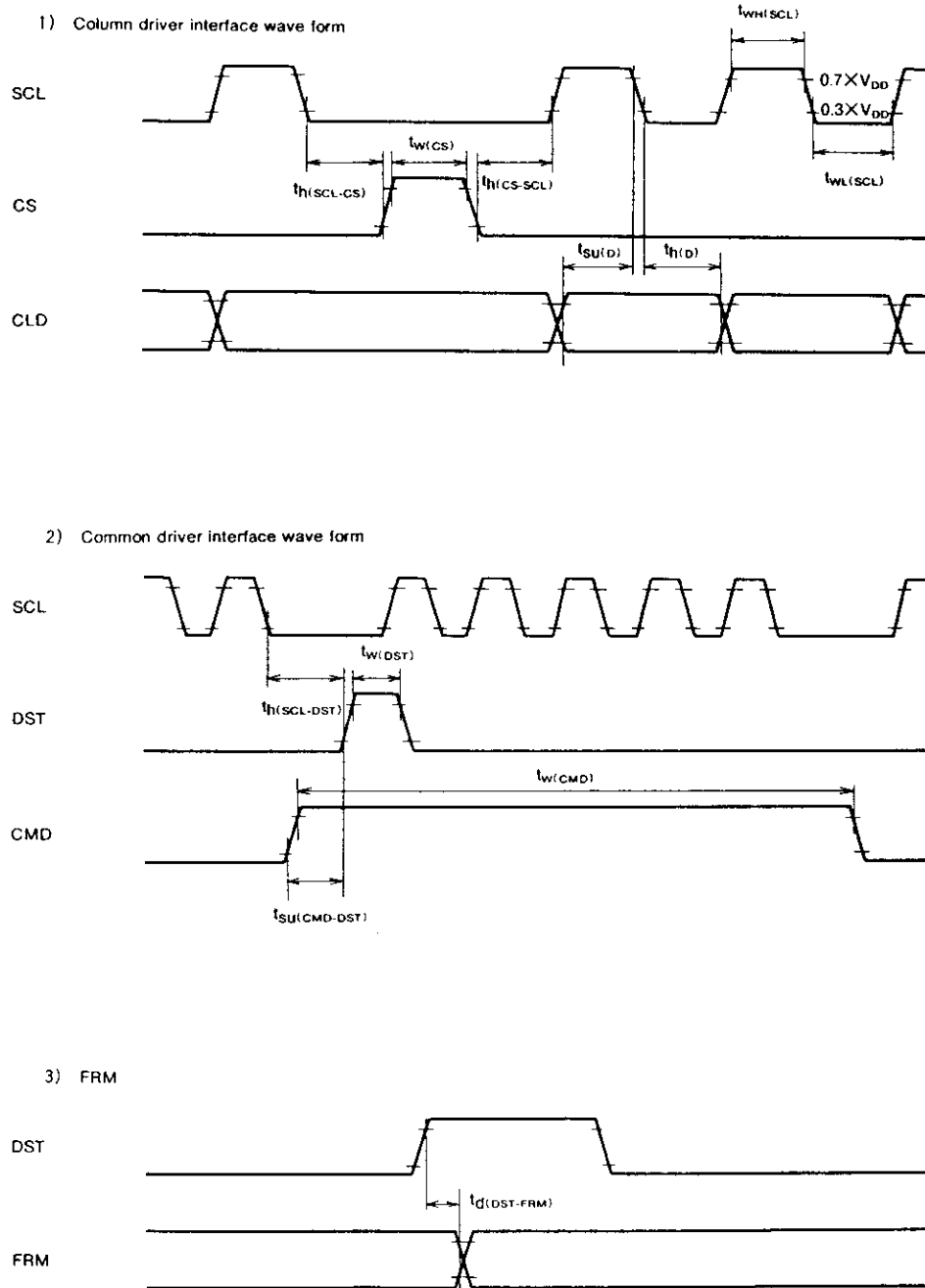


2) Write



DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

Timing Wave forms for Extended Signals



DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

Character codes and character patterns (1/2)
(example of M50530-001FP)

Character code

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F
70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F

SPACE CODE : (20)₁₆

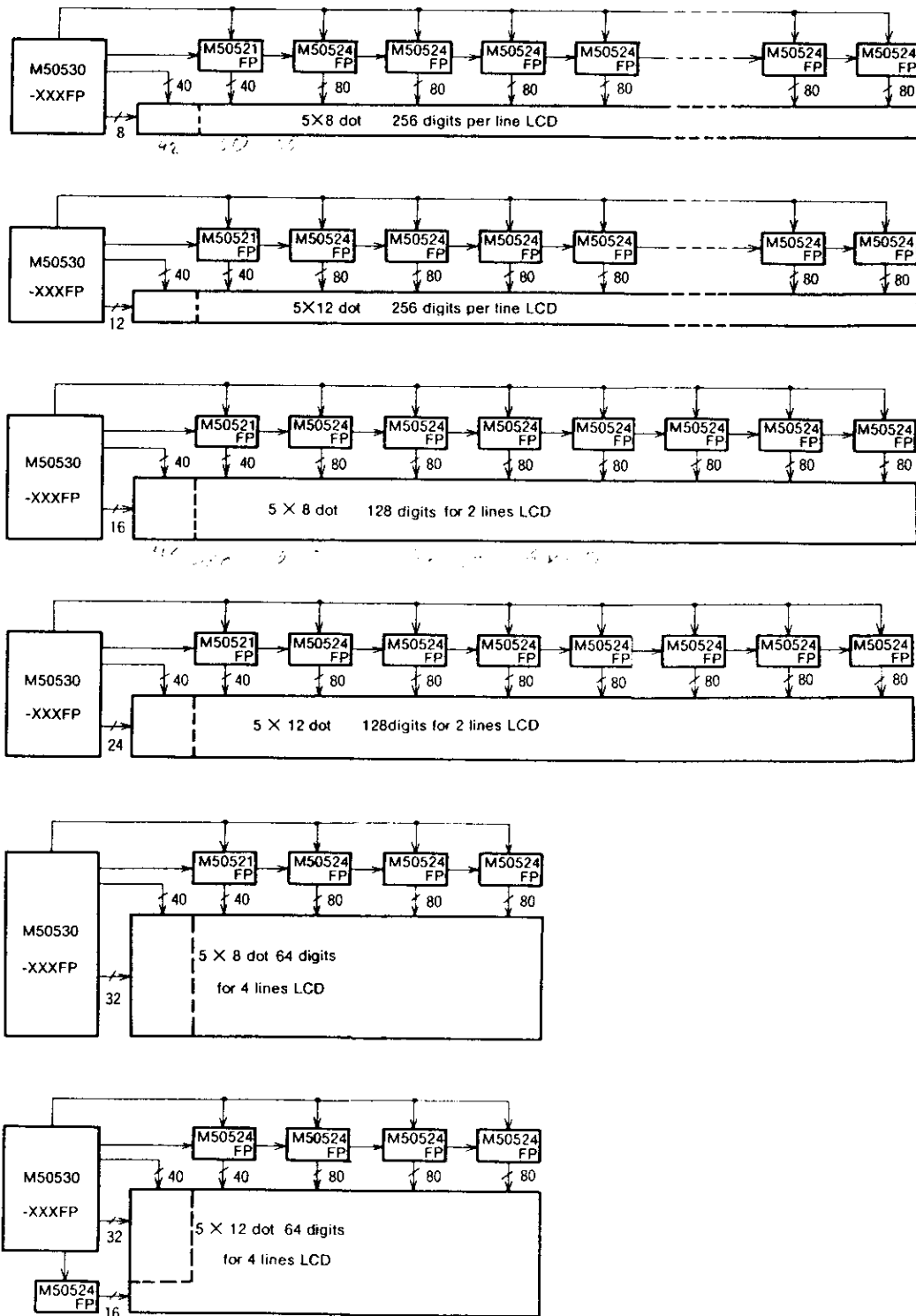
DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

Character codes and character patterns (2/2)

80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF
B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF
F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER-DRIVER

Examples of system extension (data RAM of 256 words)



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AN example of system connection

