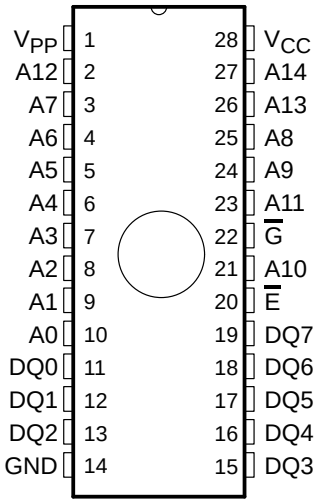
SGMS005E – MAY 1986 – REVISED JUNE 1995

- **Organization . . . 32K × 8**
- **MIL-STD-883 Class B High-Reliability Processing**
- **Single 5-V Power Supply**
- **Pin-Compatible With Existing 256K ROMs and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**
  - **'27C256-15 150 ns**
  - **'27C256-17 170 ns**
  - **'27C256-20 200 ns**
  - **'27C256-25 250 ns**
  - **'27C256-30 300 ns**
- **Power-Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming**
- **3-State Output Buffers**
- **400-mV Minimum dc Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (CMOS Input Levels)**
  - **Active . . . 165 mW Worst Case**
  - **Standby . . . 1.7 mW Worst Case**
- **Military Operating Temperature Range**
  - **– 55°C to 125°C**

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A14	Address Inputs
DQ0–DQ7	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
V_{CC}	5-V Power Supply
V_{PP}	13-V Programming Power Supply

description

The SMJ27C256 series is a set of 262 144-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pullup resistors. Each output can drive one Series 54 TTL circuit without external resistors. The data outputs are 3-state for connecting multiple devices to a common bus. The SMJ27C256 is pin-compatible with 28-pin 256K ROMs and EPROMs. It is offered in a 600-mil dual-in-line ceramic package (J suffix) rated for operation from –55°C to 125°C.

Because this EPROM operates from a single 5-V supply (in the read mode), it is ideal for use in microprocessor-based systems. One other supply (13 V) is needed for programming. All programming signals are TTL level. This device is programmable by the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations can be programmed singly, in blocks, or at random.

operation

The seven modes of operation for the SMJ27C256 are listed in Table 1. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

Table 1. Operation Modes

FUNCTION (PINS)	MODE †							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$ (22)	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X	V_{IL}	
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_{ID}	V_{ID}
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ7 (11–13, 15–19)	Data Out	Hi-Z	Hi-Z	Data In	Data Out	Hi-Z	CODE	
							MFG	DEVICE
							97	04

† X can be V_{IL} or V_{IH}.

read/output disable

When the outputs of two or more SMJ27C256s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the selected SMJ27C256, a low-level signal is applied to $\overline{E}$ and $\overline{G}$. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ0 through DQ7.

latchup immunity

Latchup immunity on the SMJ27C256 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the printed-circuit-board level when the EPROM is interfaced to industry-standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

powerdown

Active I_{CC} supply current can be reduced from 25 mA (SMJ27C256-15 through SMJ27C256-25) to 500 μA (TTL-level inputs) or 300 μA (CMOS-level inputs) by applying a high TTL/CMOS signal to the $\overline{E}$ pin. In this mode, all outputs are in the high-impedance state.

erasure

Before programming, the SMJ27C256 is erased by exposing the chip through the transparent lid to a high-intensity ultraviolet (UV) light (wavelength 2537 Å). EPROM erasure before programming is necessary to ensure that all bits are in the logic-high state. Logic lows are programmed into the desired locations. A programmed logic-low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity × exposure time) is 15 W•s/cm^2. A typical 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure; therefore, when using the SMJ27C256, the window should be covered with an opaque label.

SNAP! Pulse programming

The SMJ27C256 EPROM is programmed using the TI SNAP! Pulse programming algorithm as illustrated by the flowchart in Figure 1. This algorithm programs the device in a nominal time of 4 seconds. Actual programming time varies as a function of the programmer used.

Data is presented in parallel (eight bits) on pins DQ0 to DQ7. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte-verification step to determine when the addressed byte has been successfully programmed. Up to ten 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is completed, all bits are verified with V_{CC} = V_{PP} = 5 V.

program inhibit

Programming can be inhibited by maintaining a high-level input on $\overline{E}$.

program verify

Programmed bits can be verified with V_{PP} = 13 V when $\overline{G}$ = V_{IL} and $\overline{E}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and device type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (terminal 10); i.e., A0 = V_{IL} accesses the manufacturer code, which is output on DQ0–DQ7; A0 = V_{IH} accesses the device code, which is also output on DQ0–DQ7. All other addresses must be held at V_{IL}. Each byte contains odd parity on bit DQ7. The manufacturer code for these devices is 97h and the device code is 04h.

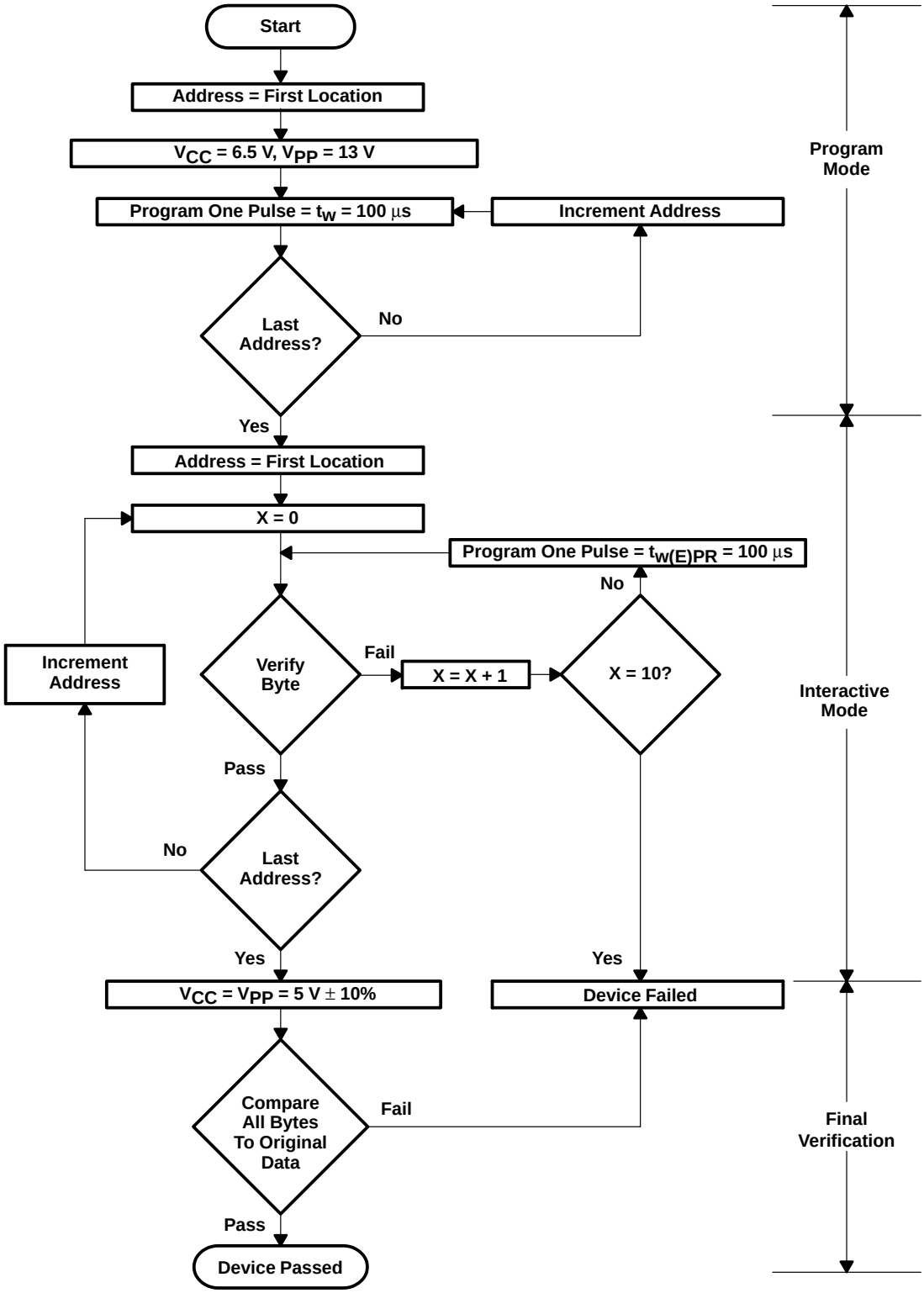
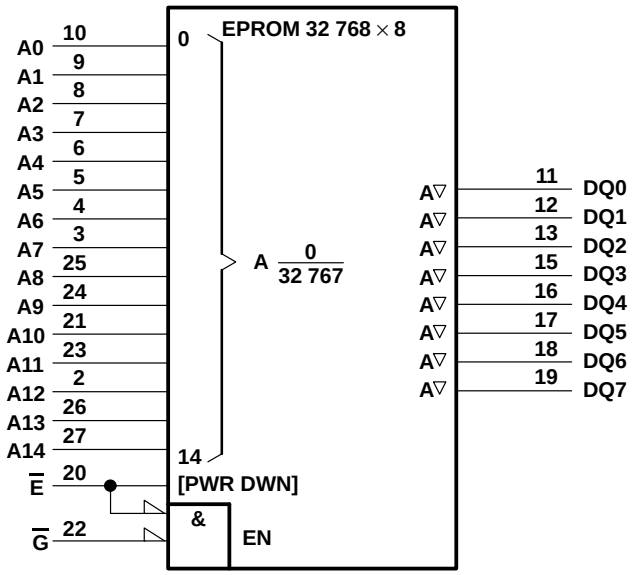


Figure 1. SNAP! Pulse Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) . . . . . –0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 . . . . . –0.6 V to 6.5 V
A9 . . . . . –0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . –0.6 V to V_{CC} + 1 V
Minimum operating free-air temperature, T_A . . . . . –55°C
Maximum operating case temperature, T_C . . . . . 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

PARAMETER				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 3)				$V_{CC}-0.6$	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level input voltage		TTL inputs	2		$V_{CC}+1$	V
			CMOS inputs	$V_{CC}-0.2$		$V_{CC}+1$	V
V_{IL}	Low-level input voltage		TTL inputs	−0.5		0.8	V
			CMOS inputs	− 0.5		0.2	V
V_{ID}	Voltage level on A9 for signature mode			11.5		13	V
T_A	Operating free-air temperature			−55			°C
T_C	Operating case temperature					125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board while V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC2} + I_{PP1}$.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −400 µA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)		V_I = 0 V to 5.5 V			±1	µA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			±1	µA
I_{PP1}	V_{PP} supply current		$V_{PP} = V_{CC}$ = 5.5 V			10	µA
I_{PP2}	V_{PP} supply current (during program pulse)‡		V_{PP} = 13 V		35	50	mA
I_{CC1}	V_{CC} supply curent (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E} = V_{IH}$			500	µA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E} = V_{CC}$			300	
I_{CC2}	V_{CC} supply current (active)	’27C256-15 ’27C256-17 ’27C256-20 ’27C256-25	V_{CC} = 5.5 V, $\overline{E} = V_{IL}$, t_{cycle} = minimum, Outputs open		15	25	mA
I_{OS}	Output short-circuit current					100	mA

† Typical values are at T_A = 25°C and nominal voltages.
‡ This parameter has been characterized at 25°C and is not tested.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V		6	10	pF
C_o	Output capacitance	V_O = 0 V		10	14	pF

† Capacitance measurements are made on a sample basis only.
‡ Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C256-15		'27C256-17		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	See Figure 2		150		170	ns
$t_{a(E)}$	Access time from $\overline{E}$			150		170	ns
$t_{en(G)R}$	Output-enable time from $\overline{G}$			70		70	ns
t_{dis}	Disable time of output from $\overline{G}$ or $\overline{E}$, whichever occurs first §		0	55	0	55	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first §		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C256-20		'27C256-25		'27C256-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	See Figure 2		200		250		300	ns
$t_{a(E)}$	Access time from $\overline{E}$			200		250		300	ns
$t_{en(G)R}$	Output-enable time from $\overline{G}$			75		100		120	ns
t_{dis}	Disable time of output from $\overline{G}$ or $\overline{E}$, whichever occurs first §		0	60	0	60	0	105	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first §		0		0		0		ns

§ Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.
NOTES: 4. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (see Figure 2).
5. Common test conditions apply to t_{dis} except during programming.

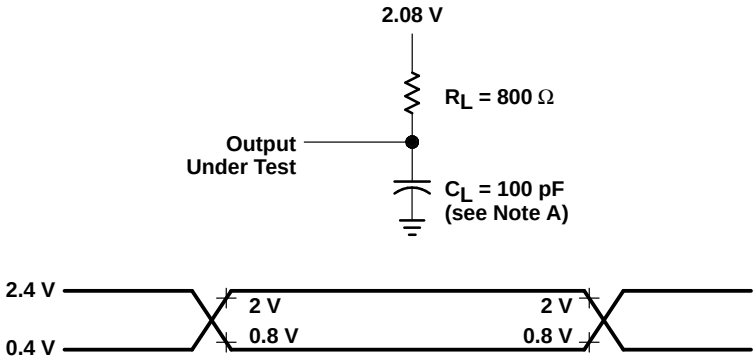
switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C

PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Output-disable time from $\overline{G}$	0	130	ns
$t_{en(G)W}$	Output-enable time from $\overline{G}$		150	ns

recommended timing requirements for programming: V_{CC} = 6.5 and V_{PP} =13 (SNAP! Pulse), T_A = 25°C (see Figure 2)

		MIN	NOM	MAX	UNIT
$t_{h(A)}$	Hold time, address	0			µs
$t_{h(D)}$	Hold time, data	2			µs
$t_{w(E)PR}$	Pulse duration, initial program	95	100	105	µs
$t_{su(A)}$	Setup time, address	2			µs
$t_{su(G)}$	Setup time, $\overline{G}$	2			µs
$t_{su(E)}$	Setup time, $\overline{E}$	2			µs
$t_{su(D)}$	Setup time, data	2			µs
$t_{su(VPP)}$	Setup time, V_{PP}	2			µs
$t_{su(VCC)}$	Setup time, V_{CC}	2			µs

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and texture capacitance
B. The ac testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

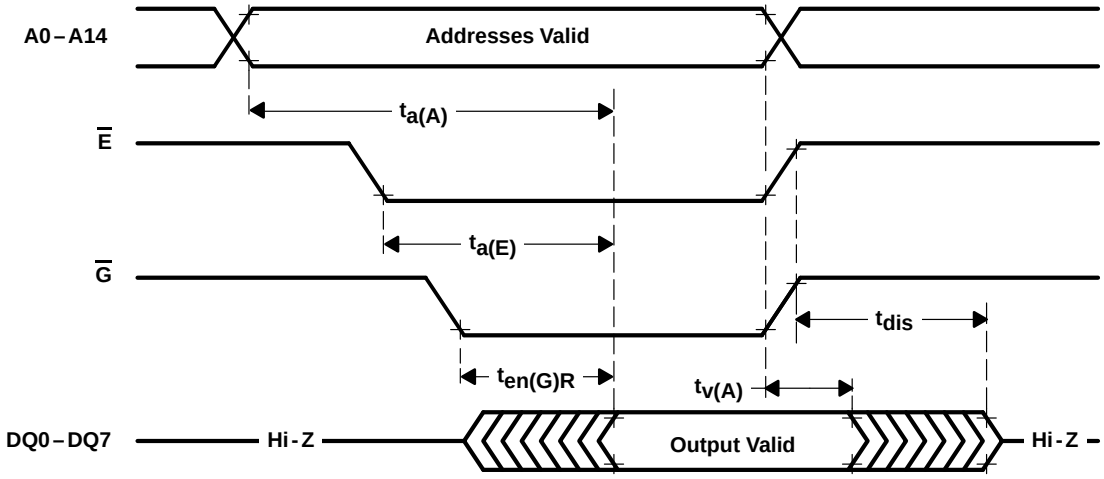


Figure 3. Read-Cycle Timing

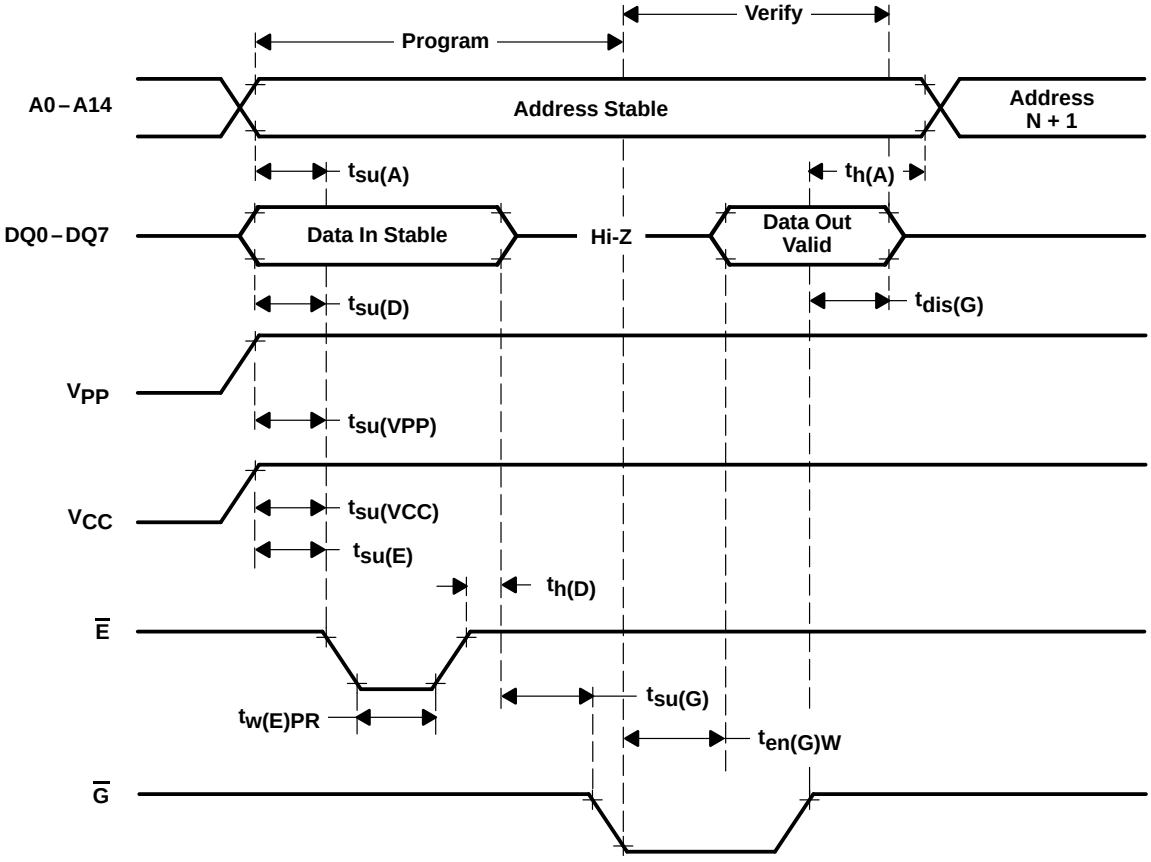
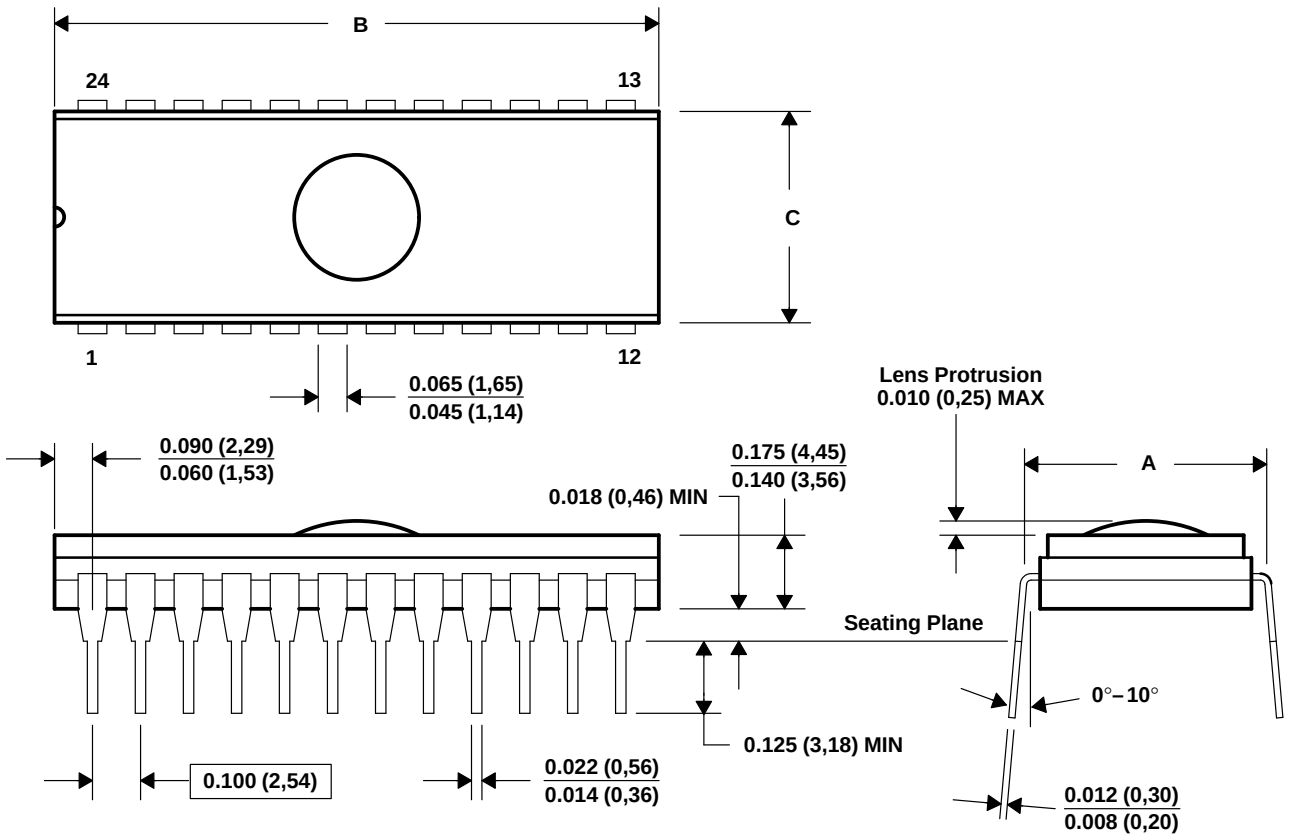


Figure 4. Program-Cycle Timing (SNAP! Pulse Programming)

MECHANICAL DATA

J (R-CDIP-T)** **CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE**

24 PIN SHOWN



DIM \ PINS**		24		28		32		40	
		NARR	WIDE	NARR	WIDE	NARR	WIDE	NARR	WIDE
A	MAX	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)
	MIN	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)
B	MAX	1.265(32,13)	1.265(32,13)	1.465(37,21)	1.465(37,21)	1.668(42,37)	1.668(42,37)	2.068(52,53)	2.068(52,53)
	MIN	1.235(31,37)	1.235(31,37)	1.435(36,45)	1.435(36,45)	1.632(41,45)	1.632(41,45)	2.032(51,61)	2.032(51,61)
C	MAX	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)
	MIN	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)

4040084/B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only

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