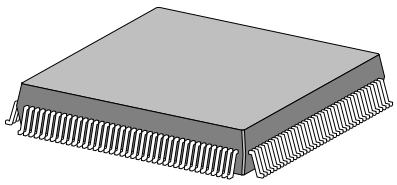
Digital Semiconductor

21150 PCI-to-PCI Bridge

Product Brief

February 1996



Description

Digital Semiconductor's 21150 is a second-generation PCI-to-PCI bridge and is fully compliant with *PCI Local Bus Specification, Revision 2.1*. The 21150 provides full support for delayed transactions, which enables the buffering of memory read, I/O, and configuration transactions. The 21150 has separate posted write, read data, and delayed transaction queues with significantly more buffering capability than first-generation bridges. In addition, the 21150 supports buffering of simultaneous multiple posted write and delayed transactions in both directions. Among the new features provided by the 21150 are: a programmable 2-level secondary bus arbiter, an IEEE standard 1149.1 JTAG interface, live insertion support, a 4-pin general-purpose I/O interface, individual secondary clock disables, and enhanced address decoding. The 21150 has sufficient clock and arbitration pins to support nine PCI bus master devices directly on its secondary interface.

The 21150 allows the two PCI buses to operate concurrently. This means that a master and a target on the same PCI bus can communicate while the other PCI bus is busy. This traffic isolation may increase system performance in applications such as multimedia.

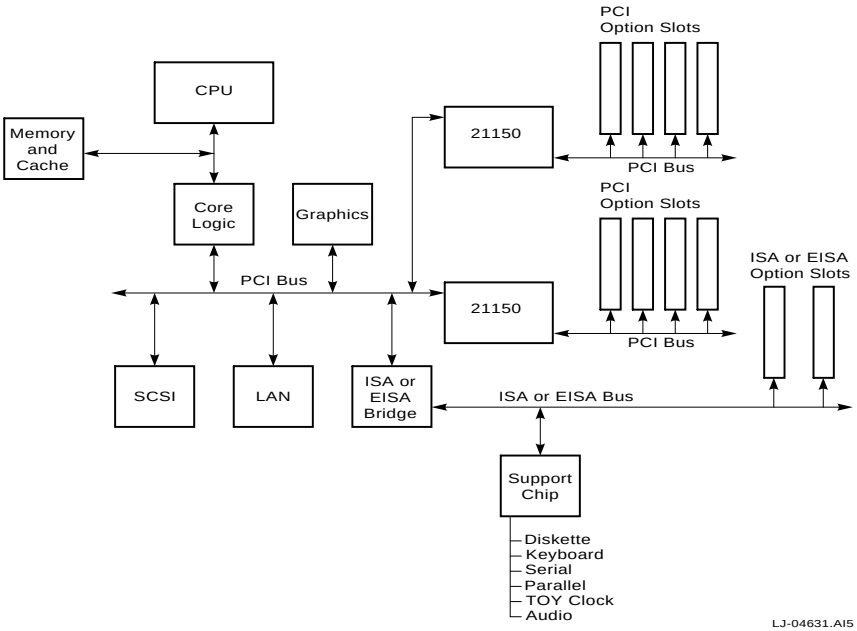
Features

- Complies fully with Revision 2.1 of the *PCI Local Bus Specification*
- Implements delayed transactions for all PCI configuration, I/O, and memory read commands—up to three transactions simultaneously in each direction
- Allows 88 bytes of buffering (data and address) for posted memory write commands in each direction—up to five posted write transactions simultaneously in each direction
- Allows 72 bytes of read data buffering in each direction
- Provides concurrent primary and secondary bus operation to isolate traffic
- Provides 10 secondary clock outputs:
  - Low skew, permitting direct drive of option slots
  - Individual clock disables are capable of automatic configuration during reset
- Provides arbitration support for nine secondary bus devices:
  - A programmable 2-level arbiter
  - Hardware disable control, permitting use of an external arbiter
- Provides a 4-pin general-purpose I/O interface, accessible through device-specific configuration space
- Provides enhanced address decoding:
  - A 32-bit I/O address range
  - A 32-bit memory-mapped I/O address range
  - A 64-bit prefetchable memory address range
  - ISA-aware mode for legacy support in the first 64KB of I/O address range
  - VGA addressing and VGA palette snooping support
- Includes live insertion support
- Supports PCI transaction forwarding for the following commands:
  - All I/O and memory commands
  - Type 1 to Type 1 configuration commands
  - Type 1 to Type 0 configuration commands (downstream only)
  - All Type 1 to special cycle configuration commands
- Includes downstream lock support
- Supports both 5-V and 3.3-V signaling environments
- Provides an IEEE standard 1149.1 JTAG interface

21150 Applications

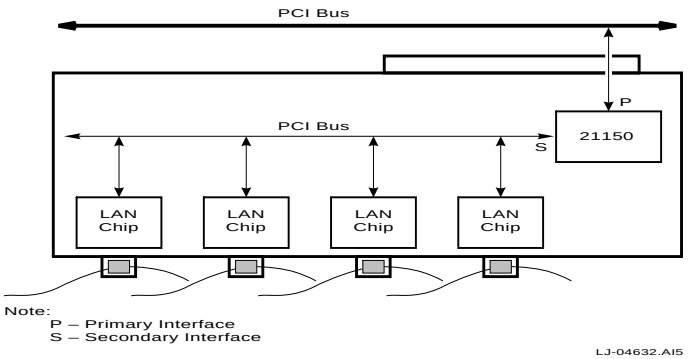
The 21150 makes it possible to extend a system's load capability limit beyond that of a single PCI bus by allowing motherboard designers to add more PCI devices, or more PCI option card slots, than a single PCI bus can support. Figure 1 illustrates the use of two 21150 PCI-to-PCI bridges on a system board. Each 21150 that is added to the board creates a new PCI bus that provides support for the additional PCI slots or devices.

Figure 1 21150 on the System Board



Option card designers can use the 21150 to implement multiple-device PCI option cards. Without a PCI-to-PCI bridge, PCI loading rules would limit option cards to one device. The *PCI Local Bus Specification* loading rules limit PCI option cards to a single connection per PCI signal in the option card connector. However, the 21150 overcomes this restriction by providing, on the option card, an independent PCI bus to which up to nine devices can be attached. Figure 2 shows how the 21150 enables the design of a multi-component option card.

Figure 2 21150 with Option Cards



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21150 Characteristics	
Characteristic	**Specification**
Power supply	**vdd**=3.3 V **vdd_clamp**=5 V or 3.3 V
Operating temperature	Tj maximum = 125°C
Storage temperature range	-55°C min, +125°C max
Power dissipation (typical)	1.2 W @ **vdd**=3.3 V with 33-MHz PCI clock
Package	208-pin PQFP

For More Information

To learn more about the availability of the 21150 and evaluation board kit, contact your local semiconductor distributor. To learn more about Digital Semiconductor's product portfolio, contact the Digital Semiconductor Information Line:

1-800-332-2717

Outside North America, call:

+1-508-628-4760

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