MICROELECTRONIC TEST STRUCTURES

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Abstract This paper reviews present day test structures and illustrates how they have evolved to a continuously changing technology. Structures for measuring resistivity, contact resistance, feature dimensions and overlay errors are presented. Test structures for helping to predict yield and Wafer Reliability Measurements (WLR) are also discussed.

1. Introduction

Microelectronic test structures are used for a wide variety of tasks which include equipment characterisation, reliability evaluations, defect monitoring, transistor parameter extraction and process verification and development. In manufacturing a small subset of these structures are normally used to confirm that the wafers have been successfully processed and can be passed over for functional test. If there are problems, then provided the appropriate test structures are available then their measurements can also be used to help identify the problem.

Early Process Control Chips PCCs consisted of test structures on small die with the contact pads situated around the edge of the chip in a similar manner to that found on product circuits. With the trend to larger circuits, and hence the opportunity to include more test structures, it became no longer feasible to access all the devices with just peripheral contact pads. With the increase in the number of test structures a point can be reached where, it becomes not only very expensive to make up the probe cards but also physically impossible. This has made it necessary, for example, to divide the chip into four identical probing patterns and step the probes internally. A more flexible approach is to use a matrix of equally spaced pads with the test devices constructed around them [1]. A 2 x N probe card can then be used to probe any device on the chip. While the use of the 2 x N type structure is very good from the point of view of flexibility it does suffer from increased testing times due to the extra prober movement required within the chip. It is for this reason that many PCCs used as drop ins do not use this approach.

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However, in recent years there has been a trend to use test structures located within the scribe channel [2]. This approach has been as a direct result of the introduction of wafer stepper technology which in most cases requires a mask change for exposing the PCC. The time taken changing over masks reduces throughput and as a result the use of dropins becomes less attractive. This approach has some advantages. It enables wafer mapping of measurements which can be used to investigate uniformity across wafers which is not possible with the dropins. Secondly in many cases it proves possible to incorporate test structures without any loss of silicon real estate thereby maximising the number of product circuits per wafer.

2. Resistivity Measurements

Resistance type measurements are a key parameter for most test structures and this section discusses the measurement of layer sheet resistances. Van der Pauw [3] developed a theory enabling the measurement of the resistivity of a continuous surface of arbitrary shape. The Greek cross [4] structure shown in figure 1 is a refinement and is ideally suited to the extraction of sheet resistance. Furthermore it is an easy structure to layout and define photolithographically. The measured sheet resistance is at the heart of the cross and an accuracy of better than 0.1% can be achieved in practice.

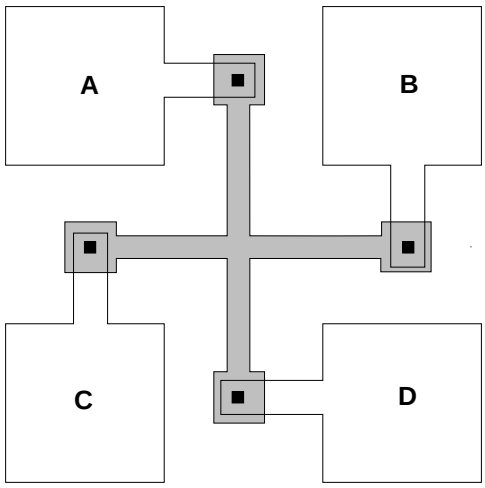

Figure 1. The Greek cross

To use the Greek cross to obtain an approximate sheet resistance (within 1%) current is passed between contacts A and B (I_{AB}) and the potential different between pads D and C (V_{DC}) measured

$$R = \frac{V_{DC}}{I_{AD}} \tag{1}$$

$$R_s = \frac{\pi R}{\ln 2} \quad \Omega/\square \tag{2}$$

The assumptions used are exactly the same as those detailed in [3]. However, in this case the current is not forced and the voltage not measured at an infinitely small point. This proves not to be a problem provided that the length of the arms is greater than or equal to the size of the heart of the cross. In this case the error from this approximation will be less than 0.1%. A more accurate measurement is to force I_{AB} and measure V_{DC}, and then reverse the current and measure the voltage V_{CD}. The resistance is then calculated as follows.

$$R_{0^\circ} = \frac{V_{DC} - V_{CD}}{I_{AB} - I_{BA}} \tag{3}$$

Current is then forced between B and C and the process repeated to give

$$R_{90^\circ} = \frac{V_{AD} - V_{DA}}{I_{BC} - I_{CB}} \tag{4}$$

The average resistance is

$$R = \frac{R_{0^\circ} + R_{90^\circ}}{2} \tag{5}$$

from which the sheet resistance can be derived.

$$R_s = \frac{\pi R}{\ln 2} \quad \Omega/\square \tag{6}$$

It is possible to evaluate parameters which illustrate the degree of asymmetry of the structure, the degree of offset in the measuring equipment and the linearity of the current voltage characteristic of the conductor [5]. The Greek cross can be used with a wafer mapping technique to allow the uniformity of an implant dose to be assessed to within 1%. Measurement currents must be kept low especially for diffused structures (<0.lmA) or silicon will show its positive TCR and surface leakage currents may affect the measurement [5].

3. Overlay and Dimensional Measurements

A design [6] which may be used for the measurement of conductor linewidth is shown in figure 2. The Greek cross at one end of the structure is used to evaluate the resistivity of the conducting layer. Current is then passed between C and D and the voltage measured between A and B. The resistance R_{AB} can then calculated from which the linewidth may be evaluated.

$$W = \frac{R_{AB}}{R_s L} \tag{7}$$

This technique can be used to measure the etch uniformity of polysilicon, metal, as well as sideways diffusion. It is sensitive to changes in dimension of ±0.1 μm provided that the width of the voltage taps are not greater than the trackwidth. This, of course, assumes that etching is uniform and that variation of sheet resistivity with position is negligible. A variant on this structure is the split cross-bridge structure [7] shown in figure 3. Although this requires a larger number of pads it has the advantage that it also extracts the pitch and so the measurement integrity can be checked.

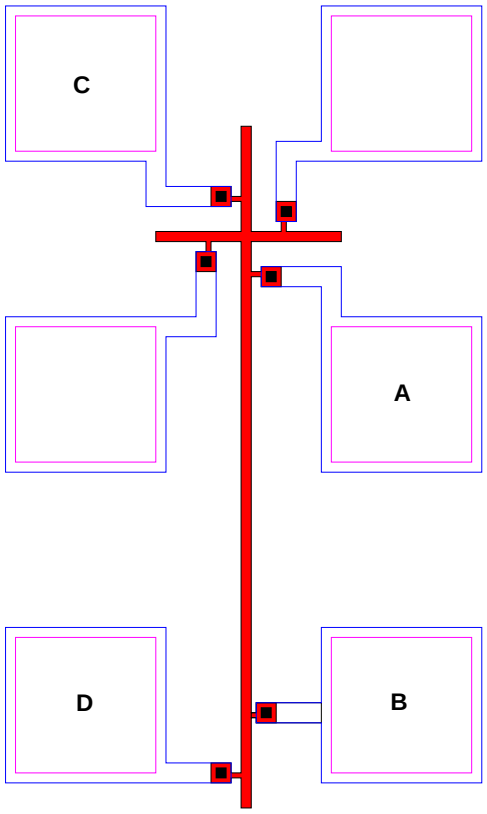

Figure 2. The cross-bridge resistor

The masks which are used in integrated circuit fabrication are aligned to one another using special patterns which are present on each mask. Alignment errors can result from incorrect stepping on the mask, faulty lithography equipment or wafer distortion. A close analysis of the spatial distribution of these errors can lead to the isolation of their source. With the reduction in device dimensions improved alignment is required and hence this type of measurement is becoming more important.

A structure [8] which can be used for measuring the overlay error between a conductor and contacts is

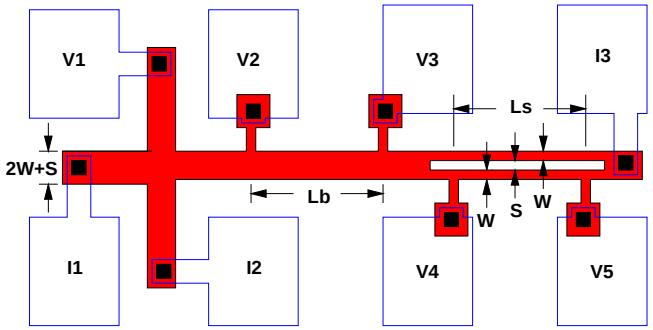

Figure 3. The split cross-bridge resistor

shown in figure 4. A current is passed between the contact pads I_1 and I_2. The voltage taps are spaced equal distances apart with V_1, V_2 and V_4 defined by the conductor mask and V_3 by the contact mask. By measuring these voltages the overlay error can be calculated in the direction of the long axis of the conducting bar. For no misalignment

$$(V_4 - V_3) = (V_3 - V_2) = (V_2 - V_1) \qquad (8)$$

The difference in voltage ΔV is given by

$$\Delta V = (V_1 - V_2) - (V_2 - V_3) \qquad (9)$$

$$\Delta V = (V_1 - V_2) - (V_3 - V_4) \qquad (10)$$

The sign of ΔV resulting from equations (9) and (10) will depend upon the direction of the overlay error. If the spacing between the taps is S the error in alignment is given by

$$e = \frac{\Delta V S}{(V_4 - V_3)} \qquad (11)$$

A similar structure at 90° will give the other component of the overlay error.

One of the errors associated with this structure is the effect that the taps have upon the effective electrical "width" of the measurement. To minimise this the tracks have traditionally been designed very much longer than the tap width. The disadvantage of this approach is that any non-uniformity in the track sheet resistance becomes incorporated in the extracted misalignment. It has been demonstrated that the resolution of the measurement can be improved significantly if the effect of the taps is accounted for [9-14]. If this is the case then the track length can be very much reduced while at the same time resistance uniformity across the structure is improved. An example of such a structure is shown in figure 5 and measurement

precision better than 10nm have been reported.

In the case of figure 5 the electrical line shortening due to the taps is given by

$$\delta l = \left(\frac{V_3 - V_4}{4V_3 + (V_3 - V_4)} \right) L_1 \qquad (12)$$

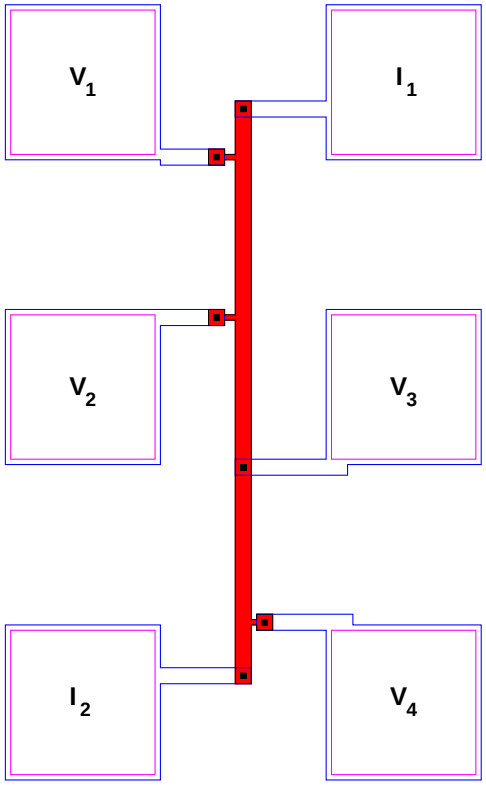

Figure 4. Structure for measuring overlay error.

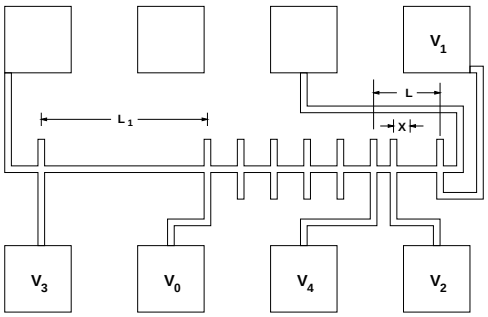

Figure 5. Structure for measuring overlay error with tap error correction.

This is then used to give the misalignment

$$X = \left(\frac{V_1 - V_2}{V_1 + V_2} \right) \left(\frac{L - 2\delta L}{2} \right) \qquad (13)$$

Figure 6 shows a schematic structure that can be adapted for measuring the misalignment between polysilicon and diffusion for a self aligned process [15]. This consists of two diffused resistors whose widths are dependent upon the degree of polysilicon misalignment (mask 2). The ratio of these two resistances gives the degree of misalignment with once again two structures at 90° being required to give both components.

Another test structure that can be used to electrically measure misalignment are vernier structures

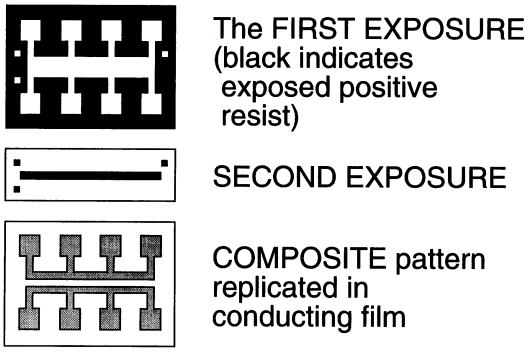

Figure 6. Schematic of structure that can be adapted for measuring the misalignment between polysilicon and diffusion for a self aligned process.

[16, 17]. These structures consist of two sets of teeth, the separation of which is based on the vernier principle. Electrical connections between them are tested, from which misalignment can be determined. The disadvantage of the vernier structure is that large numbers of pads are required [18]. Active circuits can be used to reduce the pad count in which case the structure can only function if a full process is available [16].

In-line measurements of misalignment are routinely made using optical techniques when the test structure is a box in box structure. Recently it has been proposed that holographic structures might be used to extract dimensional information [19]. Figure 7 shows the test structure pattern used to create the image of the Greek letter λ which is shown in figure 8 [20]. Research is ongoing to help select appropriate layouts to accentuate changes in the resulting image as either feature dimensions and/or misregistration between two layers change.

4. Planarisation

As Chemical Mechanical Polishing (CMP) has become more important as a planarisation technique so test structures have been introduced to help monitor uniformity. For example structures have been developed that can be used to monitor the percentage planarisation of dielectric layers [21, 22]. These use a set of capacitors with incrementally offset electrodes. Examination of the variation of capacitance with electrode overlap enables the degree of planarisation to be determined. Structures have also been proposed for monitoring CMP based Damascene process since it is widely predicted that this process will become more important in the future. To this end test structures based on the cross-bridge resistor have been used to help characterise the uniformity of CMP Damascene aluminium interconnect [23]. This set of structures can be used to monitor conductor linewidth as well as conductor thickness in order to characterise both erosion and dishing.

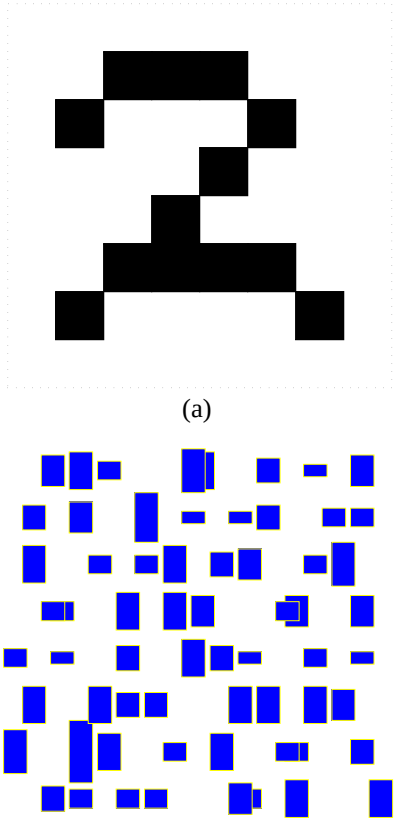

Figure 7. Holographic test structure for creating the image of the Greek letter λ. (a) Theoretical image, (b) Pattern on wafer.

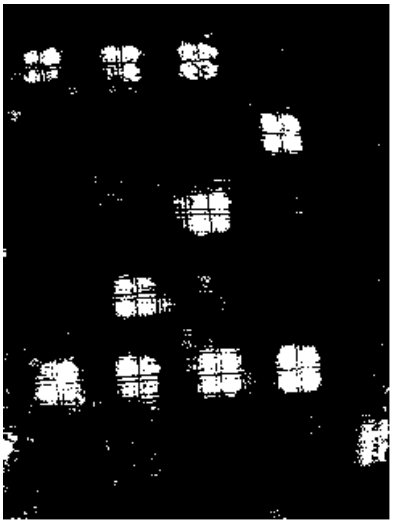

Figure 8. Image produced by layout shown in figure 7(b).

5. Contact Resistance

One of the first structures to be used to measure contact resistance between two materials was proposed by Berger [24]. One of the disadvantages of this structure is that the measurement of R_c depends upon the subtraction of two large numbers which can lead to inaccurate extractions of contact resistance. The value of R_C extracted also includes the effect of parasitic resistances and cannot take into account the change of resistivity in the diffused layer underneath the contact.

The four terminal structure of figure 9 overcomes some of these problems [25]. A current is forced between pads 1 and 3 and the voltage measured between pads 2 and 4. The current is then reversed and the measurement performed again. The voltage and current pads are then interchanged and the above measurements repeated. These four values of resistance are then averaged. This Kelvin type measurement gives the interfacial contact resistance (R_c) from which the specific contact resistivity can be derived.

$$\rho_c = R_c \; A \tag{14}$$

where A is the area of the contact [26, 27]. This assumes that the contact resistance is uniform across the whole contact area which may not always be the case [25]. References [28-31] give some details that should be considered when designing and using the Kelvin structure for measuring contact resistance.

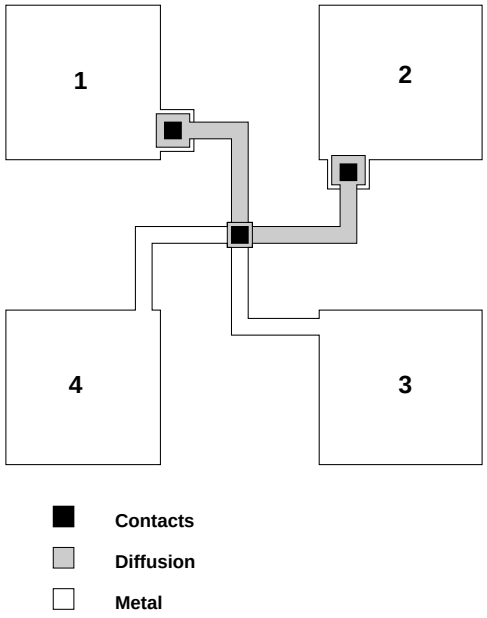

Figure 9. Kelvin structure used to measure contact resistance

6. Yield Measurements

As part of standard yield improvement programmes it is of importance to know the defect size distribution. There are many instruments available that can detect particulates on the surface of wafers. This equipment is perfectly suited to real-time measurements [32] but unfortunately it cannot differentiate between benign particulates and killer defects. Memory is ideally suited to the correlation of particulates detected by wafer scanners with those that cause electrically detectable defects. One observation from this work is that the level of correlation between defects detected during the process with killer electrical defects [32, 33] is not high. The best correlation recorded was 38% with many being about 20%. These figures are obviously very process dependent and this approach is not available when random logic devices are being fabricated. Test structures have been long used to help evaluate yield. For example, contact chains have been used [34]. These are designed to try and ensure that if they fail it is due to the contacts failing and not the interconnect between them. When an open circuit is detected there is no information available as to the size of the defect causing failure unless optical inspection is also employed. If an extra material defect were present this would manifest itself in a slightly reduced measured resistance and hence is unlikely to be detected. The first really serious attempt at electrically measuring the size of defects was by Maly [35] who used a double bridge structure layout that could extract both the type, size and density of defects landing on it. Since then Hess has used chequerboards structures in association with digital testers to extract defect data [36-40]. Satya [41] has also presented details of test structures that can be used by an adapted SEM to measure defect densities. If the yield of an IC is to be predicted then it is also essential that the Critical Area (CA) [42, 43] for each layer can be calculated together with the defect size distribution. The latest approach is to use the CA concept with test structure in an attempt to predict yield [44].

7. Wafer Level Reliability Measurements

Wafer Level Reliability (WLR) has received increasing interest in recent years. This has been a result of the requirement to built in reliability rather that using testing to remove potentially faulty devices. This has been largely achieved by using DFM techniques and SPC but this does not totally prevent rogue batches with lower reliability levels getting through to the end of the process. The purpose of WLR is to detect these wafer and ensure that potentially unreliable devices do not get deliv-

ered to the customer. This requires that measurements must be both fast, so potentially every wafer can be tested, and also ensure that the measurement does not damage the adjacent product devices. Hence, a feature of WLR devices is a source of local heat and a method of monitoring the temperature [45-47].

Examples of the types of fast WLR tests include hot carrier measurements, passivation and interconnect dielectrics, gate oxide integrity [48], in-process charging [49], mobile ions [50], SWEAT (Standard Wafer-level Electromigration Test) [51], stress migration, via voiding, current crowding and junction spiking. Accelerated tests are best suited to monitor the rate of degradation of the materials used to build the IC. With mature processes it may then be possible to correlate these measurements with lifetime predictions. It should however be remembered that if this link is to be achieved then it must be ensured that the tests are not accelerated to such a degree that the WLR structure fails from a different mechanism than that which would normally cause a failure. This is especially the case for SWEAT tests if the wafer temperature of current levels are too high [45].

WLR structures must obviously be well characterised and may be located in the scribe channel or a PCC when used to monitor production devices. The normal procedure is to first qualify the process using traditional lifetime tests. Then WRL fast tests can be used to provide a so called statistical signature of the process reliability. If the WLR measurements on product wafers show a similar distribution to those observed on the qualification lots then it can be assumed that the reliability of the devices on the wafer will be statistically similar to those observed during the qualification tests. However, if this is not the case then some other failure mechanism is probably present and the only way of ensuring reliability is to re-test using traditional reliability measurements. As reliability levels are pushed below 10 FITs it is expected that the use of WLR testing will become more important in ensuring the quality of devices reaching customers is of the desired level.

8. Equipment

The pressure on measurement equipment has increased in recent years as IC geometries and their supply voltages have reduced. Sub-pA currents and sub-μV voltages are now requiring routine measurement and the this has involved a change in the architecture of parametric test equipment. Most existing parametric test equipment has an architecture based upon that illustrated in figure 10 where the instrumentation is remote from the measurement stations.

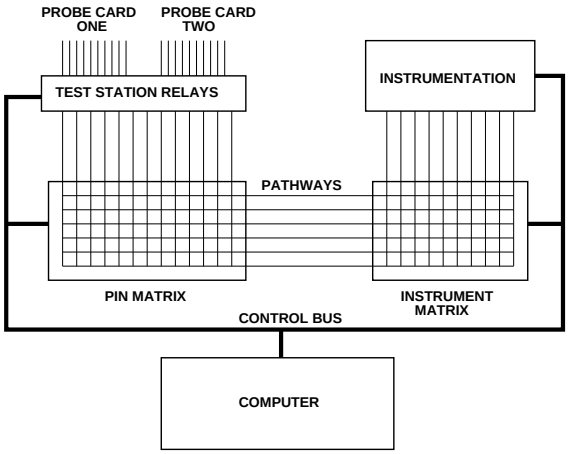

Figure 10. Traditional architecture for parametric test equipment.

This obviously makes low level measurements difficult and in addition the capacitance associated with the matrix and the relays significantly increases the measurement time. Approximate capacitances are shown in the schematic shown in figure 11.

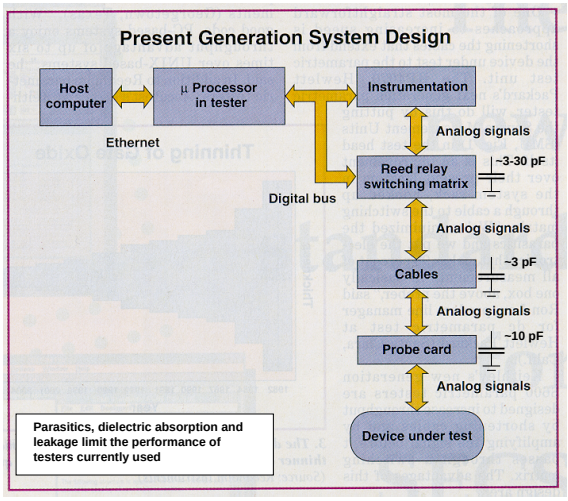

Figure 11. Schematic architecture for traditional parametric test equipment which indicates lead lengths and parasitic capacitances.

To reduce noise level and parasitic capacitances and hence speed up measurement times it is necessary to locate relays and the measurement equipment in the test head very close to the probe card. Another solution is to use pre-amplifiers in the test head to raise the signal level which has the added advantage that solid state relays can then be used for switching. This approach is illustrated in figure 12 This approach gives a 2-10 times improvement in measurement throughput since the reduce settling time resulting from the decreased capacitances. In addition the closer proximity of the measurement instru-

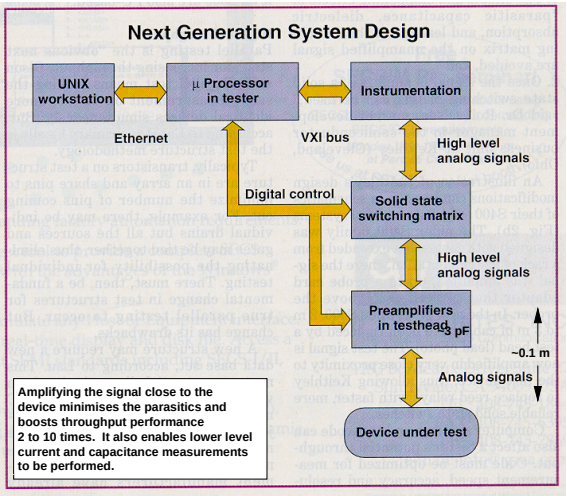

Figure 12. One of the modern architectures used for parametric test equipment.

mentation to the wafer makes lower level measurements feasible. This together with improved screening on automatic probers makes these types of measurements a reality in a production environment.

9. Conclusions

The performance of test structures has had to keep pace with technology developments as device geometries have steadily reduced. For example in 2001 feature sizes are predicted to be 180nm. Assuming that this dimension will be controlled to within 10% then a test structure will be required that has a measurement capability of at least 6nm. This paper has presented a historical perspective as to how structures for measuring dimensions and overlay errors have developed to meet these requirements. Other structures that can be used for measuring layer sheet resistance, contact resistance and defectivity measurements have been reviewed. Wafer Level Reliability (WLR) measurements have been highlighted as a growing area as there is a great desire to identify reliability problems well before devices are shipped. Test structures have developed as new processes have been established as demonstrated by the structures introduced to help monitor planarisation such as Chemical Mechanical Polishing (CMP) of oxides and damascene interconnect. Structures that can be measured using of non-contact techniques for measuring linewidth variations, misalignment and defectivity have also been presented and it is predicted that in the future this type of measurement will become more common.

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